

# Odin 13 N/V

## Alder Lake Schematic

2020-12  
REV : X01

*DY : None Installed*  
*UMA: Unified Memory Architecture*  
*OPS: Optimal Playable Settings*

0003. U15 no TPM no Psen



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Title

**Cover Page**

Size  
A4

Document Number

**Odin ADL-P**

Rev  
**X01**

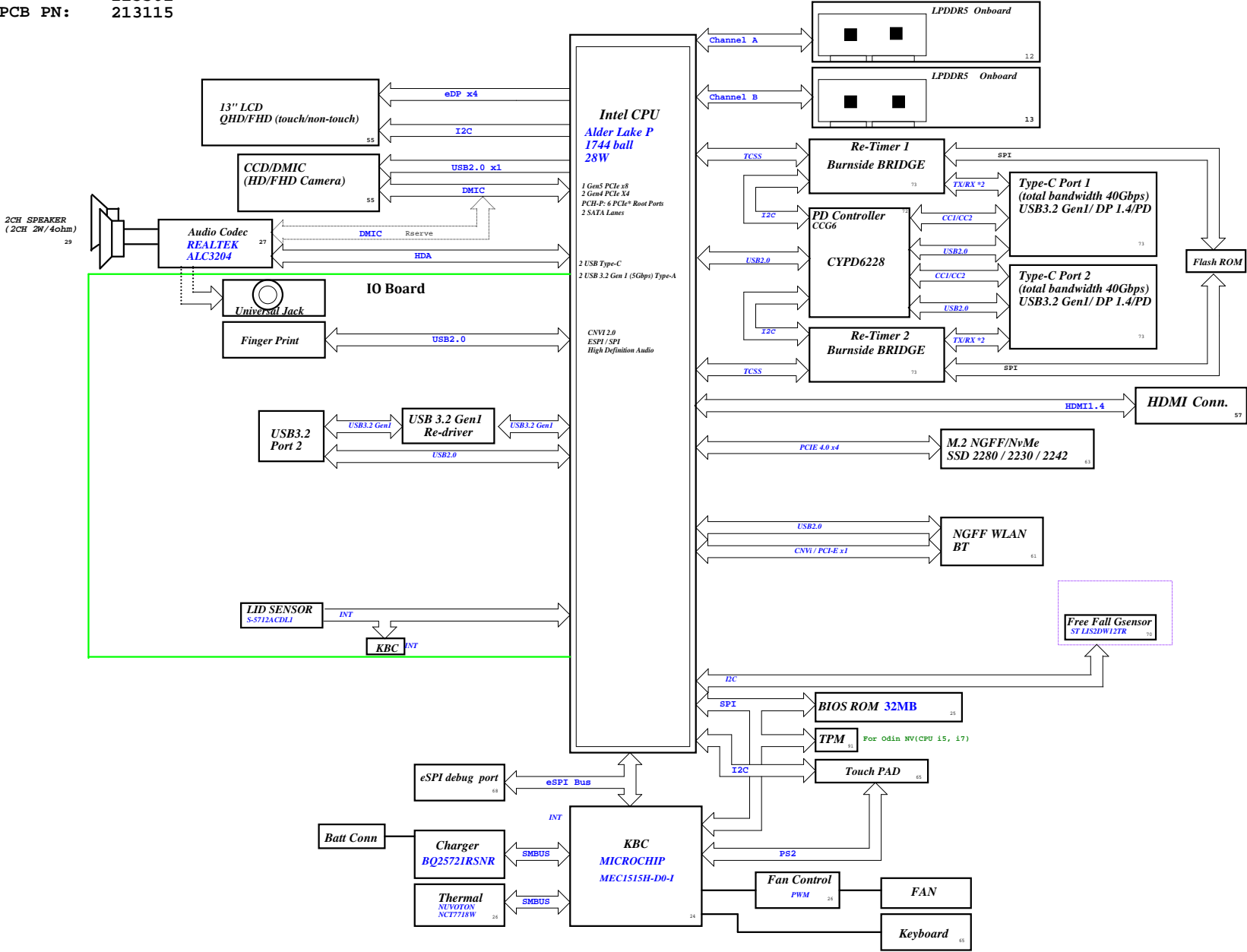
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Project name  
ODIN NV 13: 4PD0Q5010001  
MB PCB PN: 203127  
IO PCB PN: 213561  
XDP PCB PN: 213115

Odin 13 N/V ADL-P Block Diagram

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## Main Func = CPU



**Table 165. TCP Port Signal Mapping For DisplayPort\***

TCP Port Signal Mapping For DisplayPort	
Description	Signal Mapping
Main Link (Tx)	TCP_TX0 <sup>DP</sup> DP Lane_0
	TCP_TX1 <sup>DP</sup> DP Lane_2
	TCP_TXRX0 <sup>DP</sup> DP Lane_1
	TCP_TXRX1 <sup>DP</sup> DP Lane_3
Note: Apply to TCP ports only.	

TX0 <https://vinafix.com> DP Lan

Type-C #1 (TBT)

Type-C #2 (TBT)

**DESIGN NOTE:**

Stuff R404 with 2.2K for ADL P silicon

**CAD NOTE:**

TCRCOMP Resistor place as near as possible to SOC pins

### 3.7 RCOMP

The RCOMP recommendation for various interfaces provided below:

Table 29. RCOMP Recommendation

Interface	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Board parasitic capacitance (pF)	Notes
Type C	TCP_RCOMP	2.2k +/- 1% to GND	<0.015	1.4	
Display	DDIB_RCOMP	150 ohm +/-1% pull-down to GND	<0.2	-	No Cself requirement. Rdc <0.5 ohm PKG + Board
Display	DDIA_RCOMP	150 ohm +/-1% pull-down to GND	<0.15	-	No Cself requirement. Rdc <0.5 ohm PKG + Board

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Title	<b>004_CPU (DDI/EDP/TCP/DP/CSI)</b>
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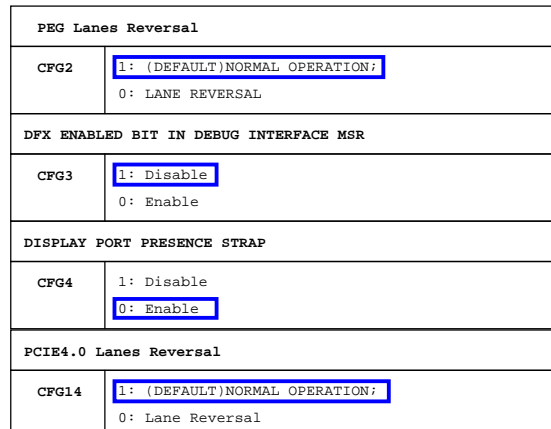
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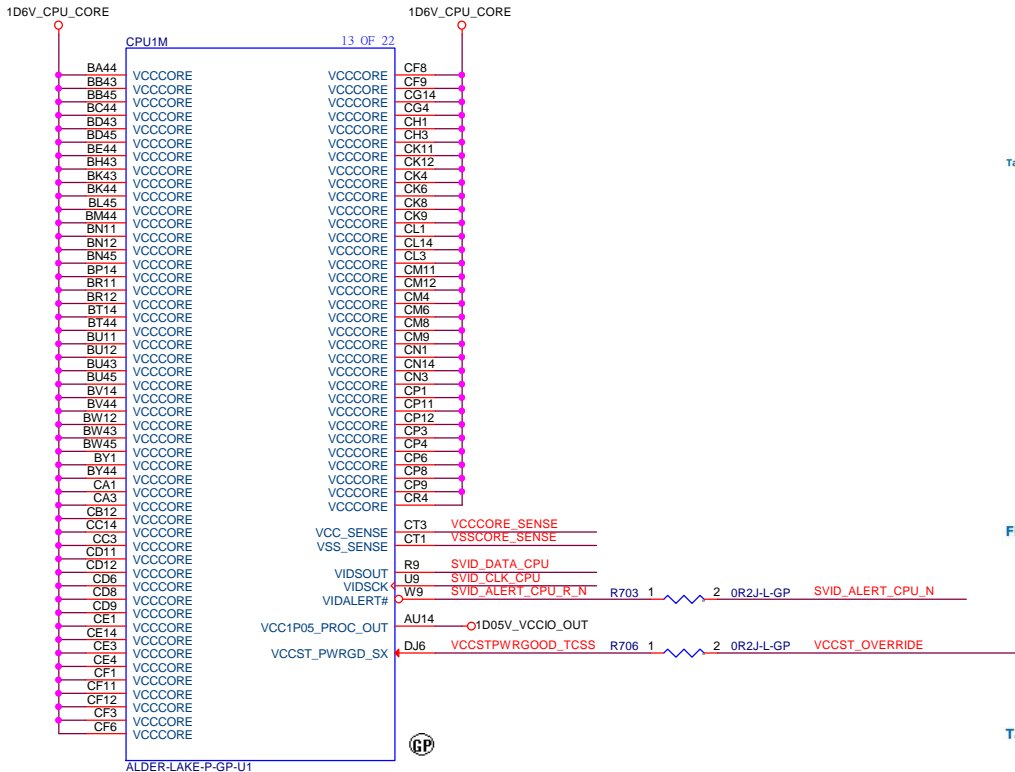
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[17:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>CFG[3:0]: Reserved configuration lanes.</li> <li>CFG[4]: eDP enable:               <ul style="list-style-type: none"> <li>1 = Disabled.</li> <li>0 = Enabled.</li> </ul> </li> <li>CFG[6:5]: Reserved configuration lanes.</li> <li>CFG[7]: PEG Training:               <ul style="list-style-type: none"> <li>1 = (default) PEG Train immediately following RESET# de assertion.</li> <li>0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>CFG[13:8]: Reserved configuration lanes.</li> <li>CFG[14]: PEG60 Lane Reversal:               <ul style="list-style-type: none"> <li>1 - (Default) Normal</li> <li>0 - Reversed</li> </ul> </li> <li>CFG[17:15]: Reserved configuration lanes.</li> </ul>	I	GTL	SE	S-Processor Line P-Processor Line
CFG_RCOMP	Configuration Resistance Compensation	NA	NA	SE	P-Processor Line continues

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<b>Title</b> <b>006_CPU (SVID/CLK/XDP/FIVR/THER)</b>			
<b>Size</b> A3	<b>Document Number</b> <b>Odin ADL-P</b>		<b>Rev</b> X01
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46 VCCORE\_SENSE <<<—  
46 VSSCORE\_SENSE <<<—  
17,40 VCCST\_OVERRIDE >>>—  
46 SVID\_ALERT\_CPU\_N >>>—  
39,46 SVID\_CLK\_CPU <<<—  
46 SVID\_DATA\_CPU <<<>>—



Layout Note:  
1. Place close to CPU within 2"  
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm  
3. Length match<25mil

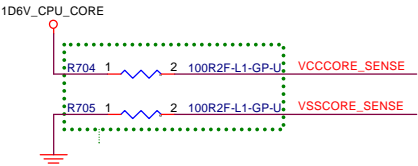


Table 750. Package Sensing Recommendations

Power Rail Sense Line	R1,R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100 Ohm	50 Ohm	<25 mils
Vccp_SENSE / Vsscp_SENSE			

Note: 1. Does not apply when rails are merged.

- To minimize any stray noise pickup to the Vcc\_SENSE/ Vss\_SENSE lines
- Sense traces should be referenced to a solid ground plane
  - Avoid crossing over plane splits
  - Maintain 25-mil separation distance away from any other dynamic signals

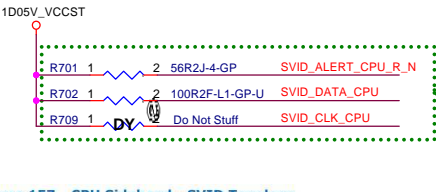


Figure 157. CPU Sideband - SVID Topology

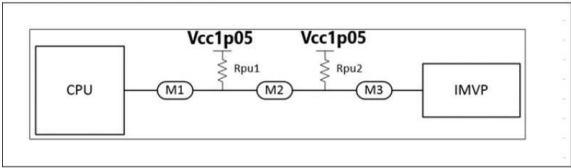



Table 341. SVID Topology Notes

Note	Detail
SVID signals	VIDSOUT, VIDSCCK, VIDSALENT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCCK platform resistors	Rpu1=Empty, Rpu2=45Ω
VIDSALENT# platform resistors	Rpu1=56Ω, Rpu2=EmptyΩ
Platform resistor tolerance	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length matching between VIDSOUT and VIDSCCK	± 2.54mm
Isolation Guidelines	Coupling length < 13mm. Spacing : MS = 125 um ; SL = 125 um. Coupling length < 65mm. Spacing : MS = 254 um ; SL = 250 um. Coupling length >65mm. Spacing : MS = 375 um ; SL = 300 um.

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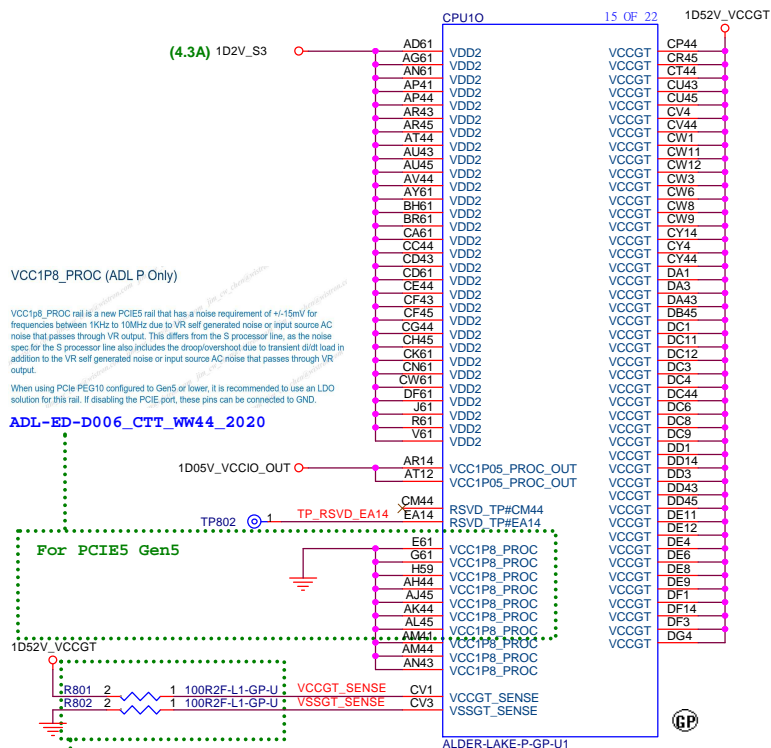
Title **007\_CPU (VCCIN)**

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## Main Func = CPU

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```
46 VCCGT_SENSE      <<<—
46 VSSGT_SENSE      <<<—
```



**Layout Note:**

1. VCCGT\_SENSE/ VSSGT\_SENSE impedance=50 ohm
2. Length match<25mil

### Table 750. Package Sensing Recommendations

Power Rail Sense Line	R1,R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100 Ohm	50 Ohm	<25 mils
VccGT_SENSE / VssGT_SENSE			
Note: 1. Does not apply when rails are merged.			

To minimize any stray noise pickup to the Vcc\_SENSE/ Vss\_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

**+VDD2\_CPU (IccMax) : 2.57A**

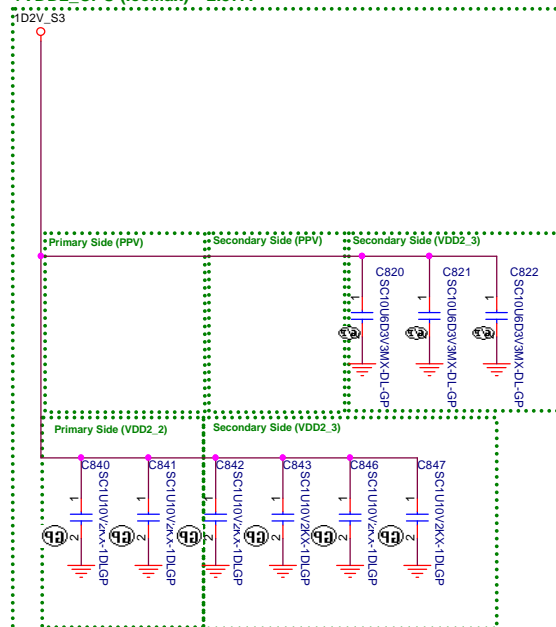


Table 770. Decoupling Solution

Design Placement	Form Factor	Value	Resistor Note	Reference Design
Primary or Secondary SMD	0402	1uF	1 Place 1uF or required value at the LDO output for stability as requires by LDO vendor or otherwise. Please ensure the design is stable	VCC1PRD_PROD
Primary or Secondary SMD	0402	150uF	1 Place directly under inverter near pin AN41. If using a single ended solution, this capacitor may be placed near pin EN3. instead.	VCC1PRD_PROD
Primary or Secondary SMD	0402	150uF	2 Place at the input of the LDO to suppress input noise between 1 to 10MHz.	VCC1PRD_PROD
Primary or Secondary SMD	0603	Phosphorizer	2 Phosphorize as shown in reference Board.	VCC1PRD_PROD

### EMC CAPS:

PLACE <4MM FROM SOC VDDQ,  
WITH EACH PAIR <12MM APART

**NOTE:**

PPV caps are for HVM testing only

Table 780. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	0402	1 uF	2	Place closer to outer edge VDD2 pins	VDD2
Secondary Side	0402	placeholder	2	Place closer to the inner row VDD2 pins	VDD2
Secondary Side	0402	10uF	3	Place closer to the inner row VDD2 pins	VDD2
Secondary Side	0402	1uF	4	Place closer to the inner row VDD2 pins	VDD2

**Table 768. Decoupling Solution**

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	0402	1uF	2	Place as close to the pins as possible	VCC1P05,

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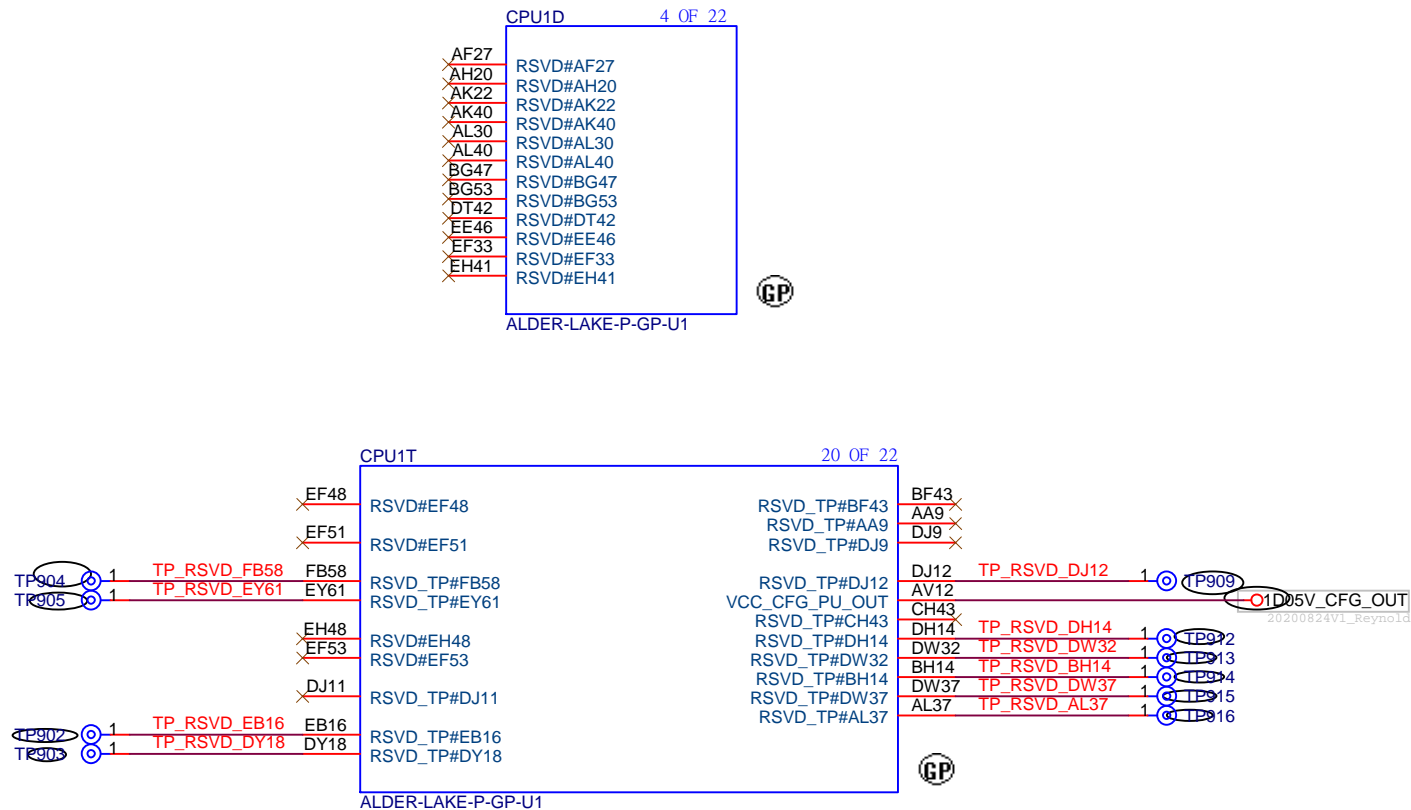
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Title	008_CPU (VCCIN_AUX/VCCST/VCCSTG
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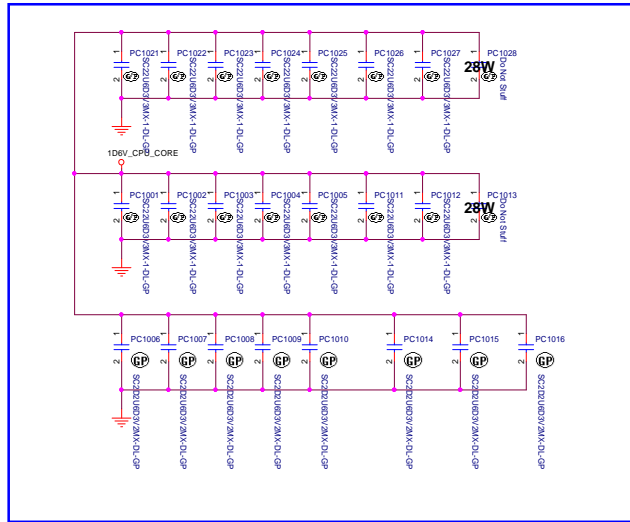
Title **009\_CPU (VSS)**

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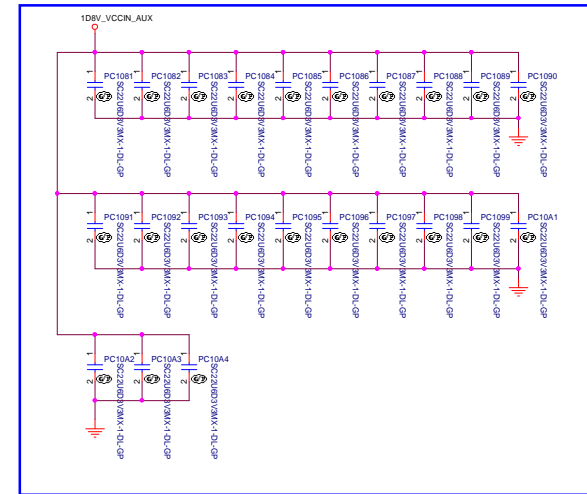
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**VCCIN** 7\*47uF 0603 + 8\*2.2uF 0402 MLCC for ADL-P U15 baseline  
8\*47uF 0603 + 8\*2.2uF 0402 MLCC for ADL-P U28 baseline

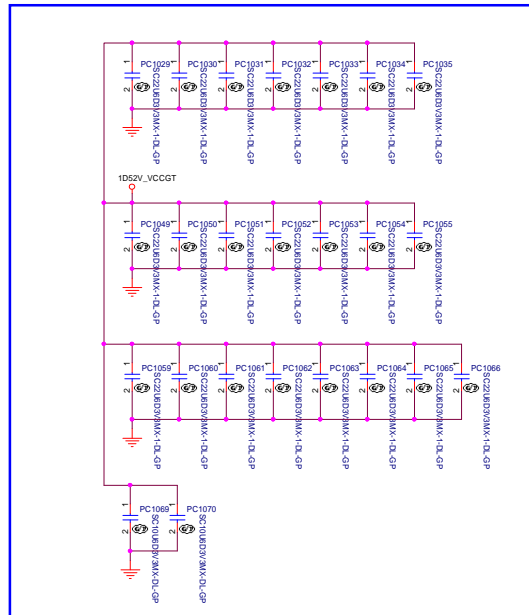
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**VCCIN\_AUX** 23\*22uF MLCC for ADL-P U28 baseline



**VCCGT** 7\*47uF + 8\*22uF + 2\*10uF MLCC for ADL-P U28 baseline




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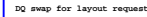
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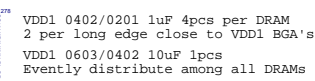
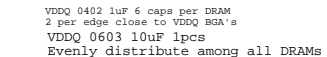
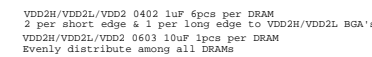
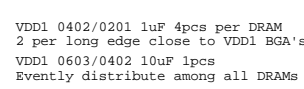
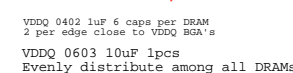
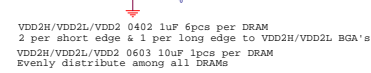
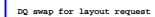
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>011_CPU (STRAP)</b>		
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Main Func = Memory

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Title <b>014_ DDR (RSVD) (DDR4-CHA1)</b>			
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GPIO	GPP_R14 Top Swap Override	SP10_MOSI	GPP_R4 JTAG ODT Disable	GPP_F0 XTAL Frequency Selection	SP10_I02 Reserved	GPP_R2 Flash Descriptor Security Override	GPP_F2 M.2 CNV1 Mode Select
Schematic							
High	Enable	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Enable Override	INTERMEDIATE CNV1 DISABLE
Low	Disable	Reserved	JTAG ODT is disabled	38.4 MHz	Reserved	Disable Override	INTERMEDIATE CNV1 ENABLE
GPIO	GPP_R19 DQPI_12C/TBT_LSS0/BIOS_LAS Pine VCC configuration	GPP_R21 DQPI_12C/TBT_LSS0/BIOS_LAS Pine VCC configuration	GPP_R10 DQPI_12C/TBT_LSS0/BIOS_LAS Pine VCC configuration	GPP_R12 DQPI_12C/TBT_LSS0/BIOS_LAS Pine VCC configuration	SP10_I03 Reserved	GPP_R18 DQPI_12C/TBT_LSS0/BIOS_LAS Pine VCC configuration	GPP_R14 Reserved
Schematic							
High	3.3V	3.3V	3.3V	3.3V	Reserved	Reserved	Enable "No Reboot" mode
Low	1.8V	1.8V	1.8V	1.8V	Reserved	Reserved	REBOOT ENABLED
GPIO	Reserved	GPP_C2 TLD Confidentiality	GPP_R23 CPUSOC Clock Frequency	GPP_F7 SPYVIOSEL SPI Operation Voltage Select	GPP_F10 Reserved	Reserved	Reserved
Schematic							
High	Reserved	Enable	19.2MHz	1.8V	NO BYPASS	Reserved	Reserved
Low	Reserved	Disable	38.4MHz	3.3V	NO BYPASS	Reserved	Reserved
GPIO	GPP_C5 Boot Strap 0	GPP_F0 Boot Strap 1	GPP_R1 Boot Strap 2	GPP_R2 Boot Strap 3	This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_R0, GPP_R1, GPP_R2 respectively). 4-bit boot strap configuration encodings: 0000 = Master Attached Flash Configuration (BIOS / CSME on SPI), eSPI is enabled 0010 = Master Attached Flash Configuration (BIOS / CSME on SPI), eSPI is disabled 0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI 1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device) 1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI Others: Reserved Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.		
Schematic							
High	Reserved	Reserved	Reserved	Reserved			
Low	Reserved	Reserved	Reserved	Reserved			

Table 16. Pin Straps

Signal	Usage	When Sampled	Comment
GPP_R14 / GPP_R19 / GPP_R21 / GPP_R23 / GPP_R25 / GPP_R27	Top Swap Override	Rising edge of PCH_PWDEN	This strap has a 20 kOhm ± 30% internal pull-down. 0 = Disable "Top Swap" mode. This results in address on access to SPI, on the alternate boot block is driven instead of the signal boot block. This PCH will revert to A0 (default) or the appropriate address from GPP_R14 is selected in the boot block on each boot. Notes: 1. The internal pull-down is disabled after PCH_PWDEN is high. 2. Software will not be able to clear the Top Swap until the system is reinitialized. 3. The value of the strap is readable using the Top Swap Register (TSR). This function is useful when running the BIOS. 4. This signal is in the primary well.
GPP_R18 / GPP_R19 / GPP_R21 / GPP_R23 / GPP_R25 / GPP_R27	No Reboot	Rising edge of PCH_PWDEN	This strap has a 20 kOhm ± 30% internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer when not in "Normal" state). This function is useful when running the BIOS. Notes: 1. The internal pull-down is disabled after PCH_PWDEN is high. 2. This signal is in the primary well.
GPP_C2 / GPP_R23 / GPP_R25	TLD Confidentiality	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = Disable Intel® CME Crypto Transport Layer Security (TLS) support when confidentiality. PCH will pull-up to 1.8V. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_C5 / GPP_R25	Boot Strap 0	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This is a 4-bit total of 4-bit encoded pin straps for boot configuration. continued...

Signal	Usage	When Sampled	Comment
GPP_R2 / GPP_R14 / GPP_R19 / GPP_R21 / GPP_R23 / GPP_R25 / GPP_R27	Flash Descriptor Security Override	Rising edge of PCH_PWDEN	This strap has a 20 kOhm ± 30% internal pull-down. 0 = Enable security override. 1 = Disable Flash Descriptor Security (default). This strap should only be asserted just before entering the BIOS. Notes: 1. The internal pull-down is disabled after PCH_PWDEN is high. 2. This signal is in the primary well.
GPP_R6 / GPP_R14 / GPP_R19 / GPP_R21 / GPP_R23 / GPP_R25 / GPP_R27	JTAG ODT Disable	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. External pull-up is recommended. 0 = JTAG ODT is disabled. 1 = JTAG ODT is enabled.
GPP_R18 / GPP_R19 / GPP_R21 / GPP_R23 / GPP_R25 / GPP_R27	NO BYPASS	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = DQPI_12C / TBT_LSS0 / BIOS_LAS pins at 1.8 V 1 = DQPI_12C / TBT_LSS0 / BIOS_LAS pins at 3.3 V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_R21 / GPP_R23 / GPP_R25	DQPI_12C / TBT_LSS0 / BIOS_LAS pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = DQPI_12C / TBT_LSS0 / BIOS_LAS pins at 1.8 V 1 = DQPI_12C / TBT_LSS0 / BIOS_LAS pins at 3.3 V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
DBL_PWDEN	Reserved	Rising edge of RSMRST#	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

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Signal	Usage	When Sampled	Comment
GPP_C7	Reserved	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F0 / GPP_F10 / GPP_R25	XTAL Frequency Selection	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = 38.4 MHz (default) 1 = 24 MHz Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F2 / GPP_R25	M.2 CNV1 Mode Select	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0 = Integrated CNV1 disabled. 1 = Integrated CNV1 enabled. Note: When CNV1 companion chip is connected to the PCH, CNV1 interface, the device internal pull-down resistor will pull the device down to VCCDDN_CNV1 level. continued...

Signal	Usage	When Sampled	Comment
GPP_F7	Reserved	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F10	Reserved	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_R0	Boot Strap 1	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This is a 4-bit total of 4-bit encoded pin straps for boot configuration. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_R1	Boot Strap 2	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This is a 4-bit total of 4-bit encoded pin straps for boot configuration. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_R2	Boot Strap 3	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. This is a 4-bit total of 4-bit encoded pin straps for boot configuration. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_R23 / GPP_R25 / GPP_R27	CPUSOC Clock Frequency	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = 19.2 MHz clock (default) 1 = 38.4 MHz clock (default from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as RSMRST# and strap low, a 150 K pull-up is needed in order to not correct the internal pull-down strap sampling. 3. This signal is in the primary well.
SP10_I02	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommended 100K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SP10_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommended 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. continued...

42617-011-g-pub-04-01-001-001

GPIO	GPP_R14/GPP_R19 TOP SWAP OVERRIDE	SP10_MOSI	GPP_R4 JTAG ODT Disable	GPP_F0 XTAL Freq Selection	SP10_I02 SPI_NP_CNV1	GPP_R2 / GPP_R14 Flash Security Override	GPP_F2 / GPP_R25 M.2 CNV1 Mode Select
Schematic							
High	Enable	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Enable Override	INTERMEDIATE CNV1 DISABLE
Low	Disable	Reserved	JTAG ODT is disabled	38.4 MHz	Reserved	Disable Override	INTERMEDIATE CNV1 ENABLE
GPIO	GPP_R19/CNV1 Pine VCC config	GPP_R21/CNV1 Pine VCC config	GPP_R10/CNV1 Pine VCC config	GPP_R12/CNV1 Pine VCC config	GPP_R18/CNV1 Pine VCC config	GPP_R14/CNV1 Pine VCC config	GPP_R14/CNV1 Pine VCC config
Schematic							
High	3.3V	3.3V	3.3V	3.3V	Reserved	Reserved	Enable "No Reboot" mode
Low	1.8V	1.8V	1.8V	1.8V	Reserved	Reserved	REBOOT ENABLED
GPIO	GPP_C7 Boot Strap 0	GPP_F0/GPP_R1 Boot Strap 1	GPP_R2/GPP_R1 Boot Strap 2	GPP_R2/GPP_R1 Boot Strap 3	GPP_R2/GPP_R1 Boot Strap 3	GPP_R2/GPP_R1 Boot Strap 3	GPP_R2/GPP_R1 Boot Strap 3
Schematic							
High	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Low	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved









Main Func = PCH

27.96 HDA\_SDOUT\_CODEC <<<--  
27 HDA\_SYNC\_CODEC <<<--  
15.19 HDA\_BITCLK\_CODEC <<<--  
27.96 HDA\_SDOUT\_CPU <<<--  
27.96 HDA\_SDOIN0\_CPU <<<--

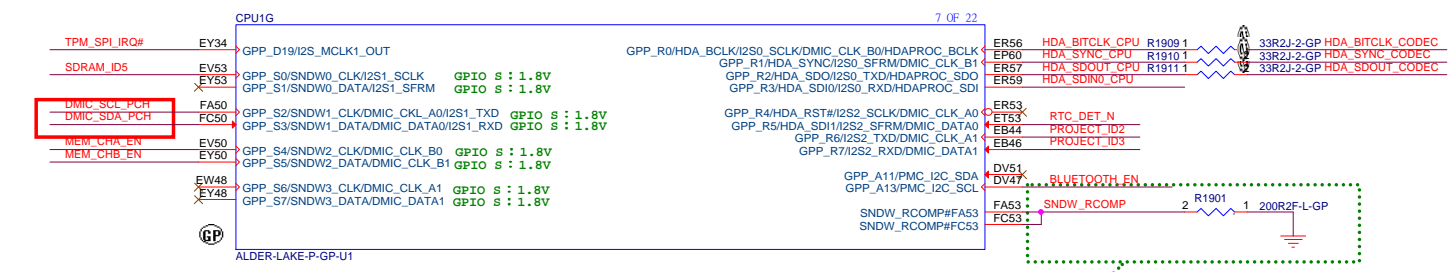
21 SDRAM\_ID5 >>>--  
21 PROJECT\_ID2 >>>--  
21 PROJECT\_ID3 >>>--  
21 MEM\_CHA\_EN >>>--  
21 MEM\_CHB\_EN >>>--

25 RTC\_DET\_N >>>--  
61 BLUETOOTH\_EN <<<--  
15.19 HDA\_SDOUT\_CPU >>>--

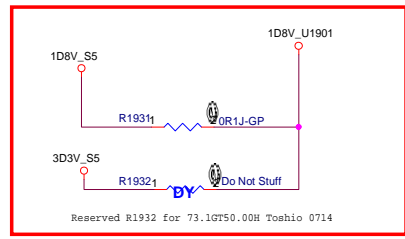
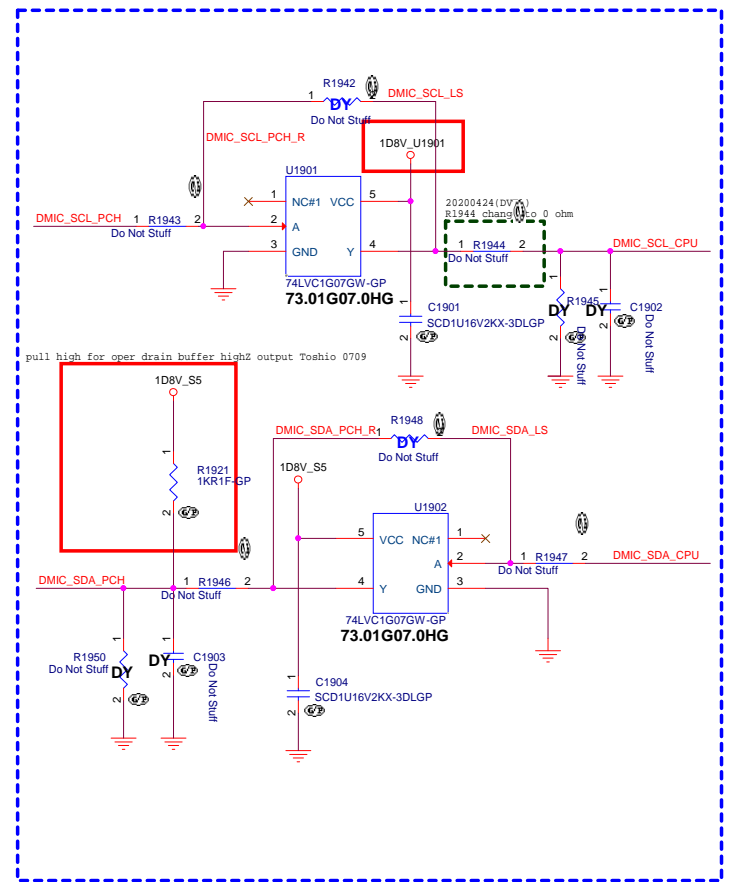
91 TPM\_SPI\_IRQ# <<<--

SIV Auto Test

96 HDA\_BITCLK\_CPU >>>--



Soundwire	SNDW_RCOMP	200ohm +/- 1% to GND	0.1	-	
-----------	------------	----------------------	-----	---	--



16.2.1 Configurable GPIO Voltage

Except for all pads in GPIO S, GPIO R, and GPD groups, all other GPIO groups support per-pad configurable voltage, which allows control selection of 1.8 V or 3.3 V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8 V level with 3.3 V tolerant.
- Output: the pin drives 3.3 V via a ~20 K pull-up. With this, any 1.8 V device must be capable of taking 20 K pull-up to 3.3 V.


WARNING

GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

NOTES

1. GPIO S group supports 1.8 V only.
2. GPIO R group supports per-group voltage configuration (3.3 V or 1.8 V) only.
3. GPD group supports 3.3 V only.

0003. U15 no TPM no Psen

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

**019\_PCH (CLK/CNVI)**

Size Custom Document Number **Odin ADL-P** Rev **X01**

Date: Friday, August 06, 2021 Sheet 19 of 105

Main Func = PCH

DUDC DEBUG

ESPI DEBUG

68 CPU\_UART\_TXD  
68 CPU\_UART\_RXD

eDP (Touch Panel)

Touch Pad

65,66 CPU\_I2C\_SCL\_TP  
65,66 CPU\_I2C\_SDA\_TP

65 KB\_LED\_BL\_DET

24,66,67 LID\_CL\_SIO#

71,75 TBT\_FORCE\_PWR

G-Sensor

66 CPU\_I2C\_SCL\_GSENSOR  
66 CPU\_I2C\_SDA\_GSENSOR

70 GSEN2\_INT1\_C

70 GSEN2\_INT2\_C

24 TABLE\_MODE#

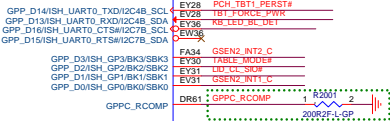
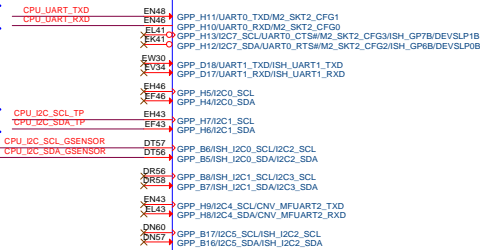
71,75 PCH\_TBT1\_PERST#

SATA LED

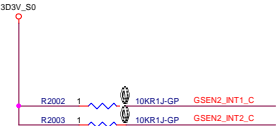
24,64 MASK\_SATA\_LED#

ESPI DEBUG

E3 Touch Pad Accelerometer



GPIO	GPPC_RCOMP	200 ohm +/-1% pull-down to GND	-	-	
------	------------	--------------------------------	---	---	--



https://vinafix.com



**Main Func = PCH**

<https://vinafix.com>

## CNVi

```

61  CNV_WT_DP1      <<<<<
61  CNV_WT_DN1      <<<<<
61  CNV_WT_DP0      <<<<<
61  CNV_WT_DN0      <<<<<
61  CNV_WT_CLKP     <<<<<
61  CNV_WT_CLKN     <<<<<

61  CNV_WR_DP1      <<<<<
61  CNV_WR_DN1      <<<<<
61  CNV_WR_DP0      <<<<<
61  CNV_WR_DN0      <<<<<
61  CNV_WR_CLKP     <<<<<
61  CNV_WR_CLKN     <<<<<

61  CNV_RF_RST_N    <<<<<
61  CNV_BRI_RSP_PCH <<<<<
61  CNV_RGI_RSP_PCH <<<<<
15,61 CNV_RGI_DT_PCH <<<<<
15,61 CNV_BRI_DT_PCH <<<<<
61  CNV_CLKREQ      <<<<<

```

```

18  SDRAM_ID0  < < < —
18  SDRAM_ID4  < < < —
19  SDRAM_ID5  < < < —

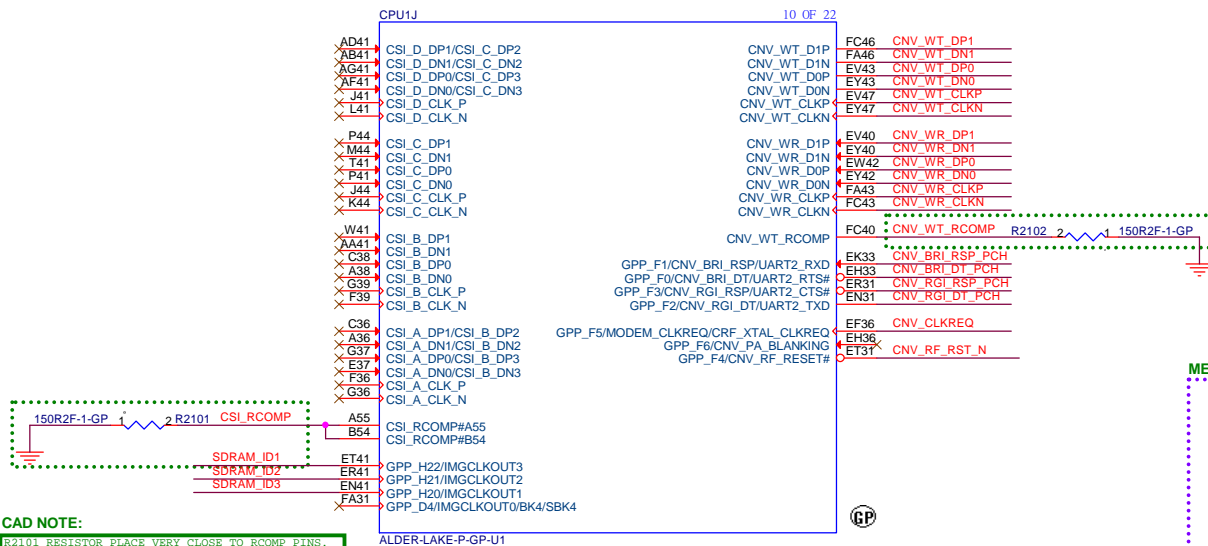
```

```
19 PROJECT_ID2 <<<=
19 PROJECT_ID3 <<<=
```

```

19  MEM_CHA_EN< < < —
19  MEM_CHB_EN< < < —
    MEM_SPEED_SEL< < < —

```

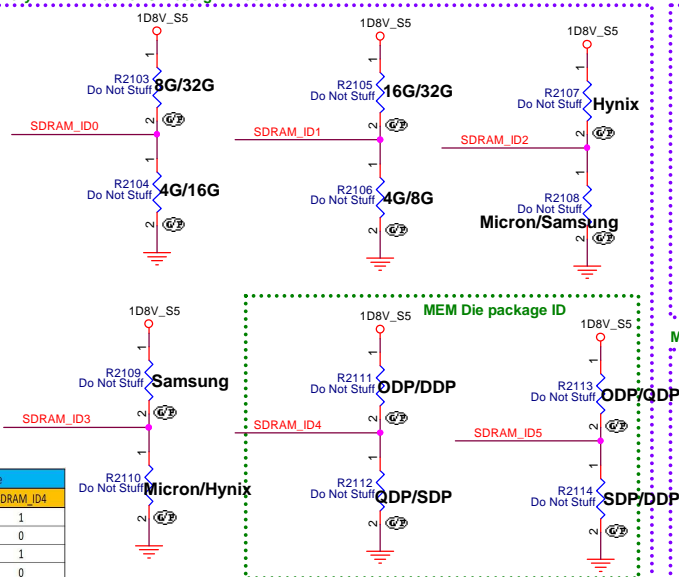
18 TBT\_DET#<<<—18 P\_SENSOR\_DET <>—

**CAD NOTE:**

R2101 RESISTOR PLACE VERY CLOSE TO RCOMP PINS.  
FOLLOW THE PDG GUIDELINES

Imaging	CSI_RCOMP	150 ohm +/-1% pull-down to GND	<0.5	-	No Cself requirement. Rdc <0.5 ohm Pkg + Board
PCH interface	CNV_RCOMP	150 ohm +/-1 % pull-down to GND	<0.5	-	Pkg trace + Board trace <1pf should be sufficient

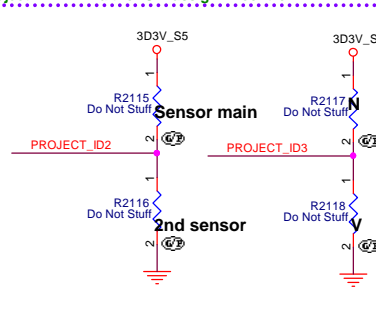
**Memory ID PIN: Wait for SW assign ID control**



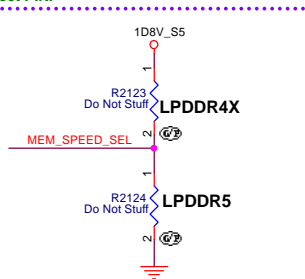
Odin13 Memory ID LPDDR5		Die package	
Vendor	Capacity	SDRAM_ID5	SDRAM_ID4
SDP/DDP/QDP/QDP config	ODP	1	1
	QDP	1	0
	DDP	0	1
	SDP	0	0

Qdix13 Memory ID: LPD105		Vendor				Capacity
Vendor	Capacity	SDRAM ID3	SDRAM ID2	SDRAM ID1	SDRAM ID0	
Micron	4GB	0	0	0	0	
	8GB	0	0	0	1	
	16GB	0	0	1	0	
	32GB	0	0	1	1	
Hynix	4GB	0	1	0	0	
	8GB	0	1	0	1	
	16GB	0	1	1	0	
	32GB	0	1	1	1	
Samsung	4GB	1	0	0	0	
	8GB	1	0	0	1	
	16GB	1	0	1	0	
	32GB	1	0	1	1	

**Project ID PIN: Wait for SW assign ID control**

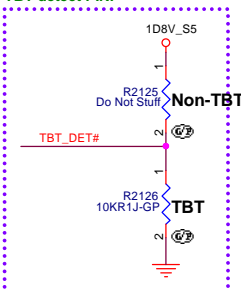


**MEM Speed Select PIN:**



GPIO	Net name	Voltage	Note
GPP_S7	SDRAM_ID0	1.8V	Capacity
GPP_H22	SDRAM_ID1	1.8V	Capacity
GPP_H21	SDRAM_ID2	1.8V	Vendor
GPP_H20	SDRAM_ID3	1.8V	Vendor
GPP_S6	SDRAM_ID4	1.8V	TBD
GPP_S0	SDRAM_ID5	1.8V	TBD

TBT detect PIN:



ID	Description	Setting	Mapping
MEM_Speed SEL	Speed Configuration	1	LPDDR4X
		0	LPDDR5

0003, U15 no TPM no Pser



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>021 PCH (SDW/HDA/ISH/GPIO)</b>
-------	-----------------------------------

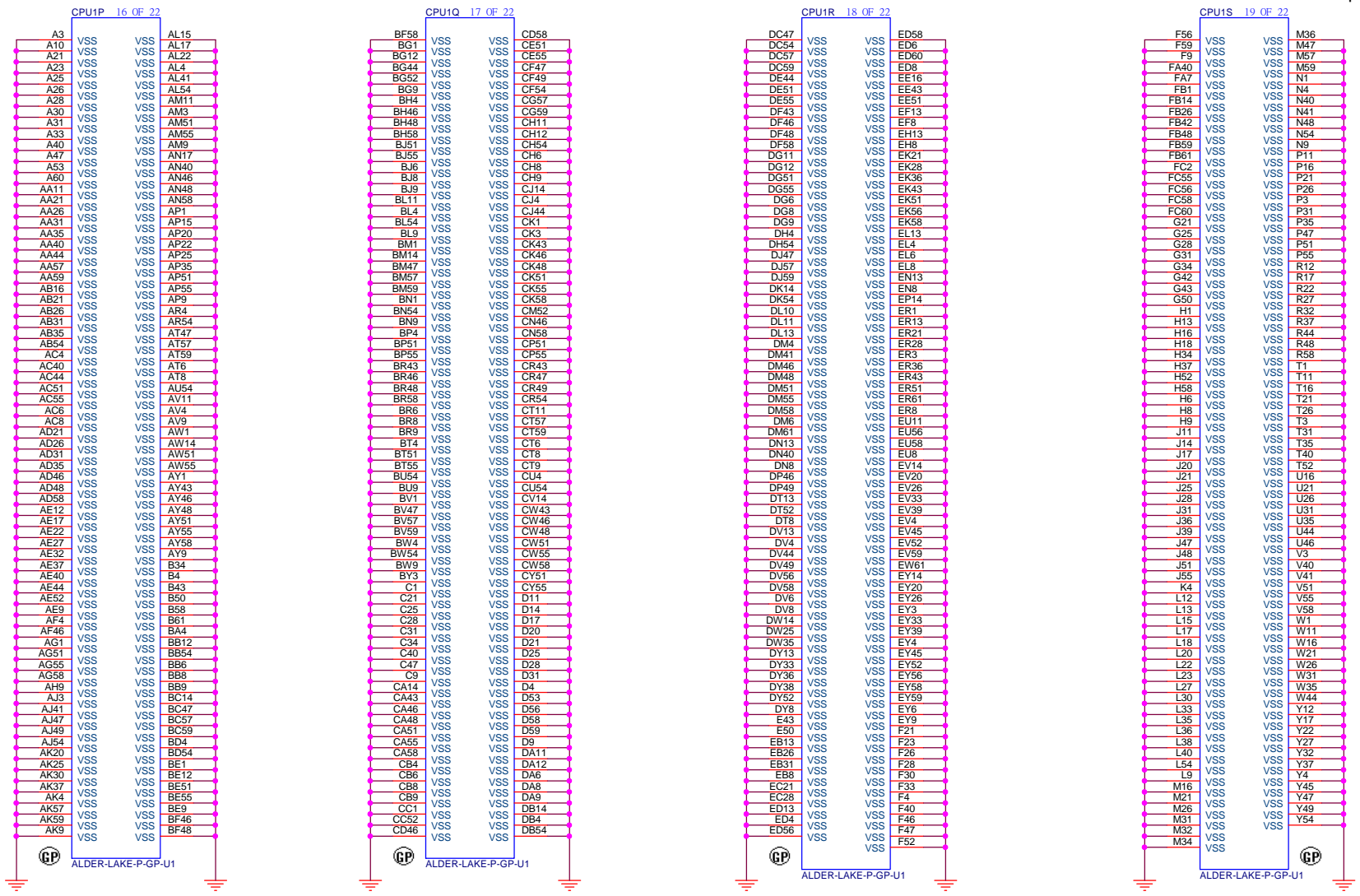
Size A3	Document Number <b>Odin ADL-P</b>	Rev <b>X0</b>
Date: Friday, August 06, 2021	Sheet 21 of 105	

Odin13 Project ID	P sen	NON Psen
P_SENSOR_DET	1	0



Main Func = PCH

https://vinafix.com





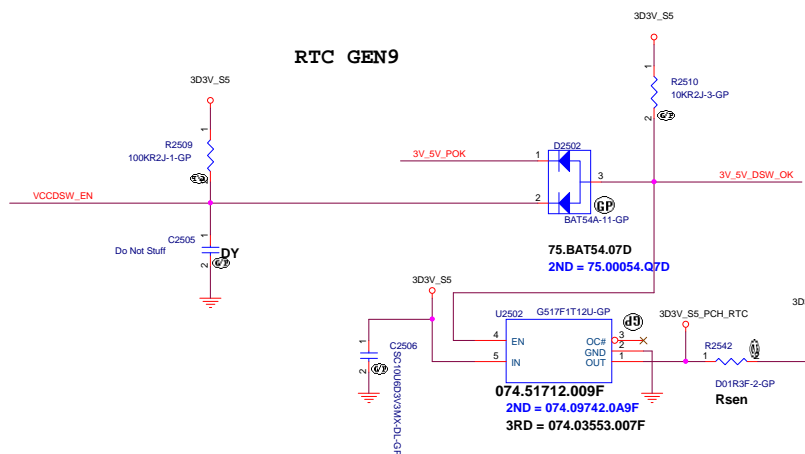
# SSID = Flash.ROM SPI FLASH ROM (32M byte) for PCH

18,24,68 SPI\_CS\_CPU\_N0 >>> \_\_\_\_\_  
 18,24,68,91 SPI\_SO\_ROM <<< \_\_\_\_\_  
 18,24,68 SPI\_WP\_ROM <<> \_\_\_\_\_  
 18,24,68 SPI\_HOLD\_ROM << \_\_\_\_\_  
 18,24,68,91 SPI\_CLK\_ROM >>> \_\_\_\_\_  
 18,24,68,91 SPI\_SI\_ROM >>> \_\_\_\_\_

19 RTC\_DET\_N <<< \_\_\_\_\_  
 24 RTCRST\_ON >>> \_\_\_\_\_  
 24 VCCDSW\_EN >>> \_\_\_\_\_  
 17,25,45 3V\_5V\_POK >>> \_\_\_\_\_  
 17,25,45 3V\_5V\_POK <<< \_\_\_\_\_

Main Func = RTC

## RTC GEN9



Used SOP8 footprint, BOM used WSON8  
 Co-lay with SPI25 reserved socket for BIOS update

32M NON RPMC WSON8

072.25673.0003

072.25256.0AB1

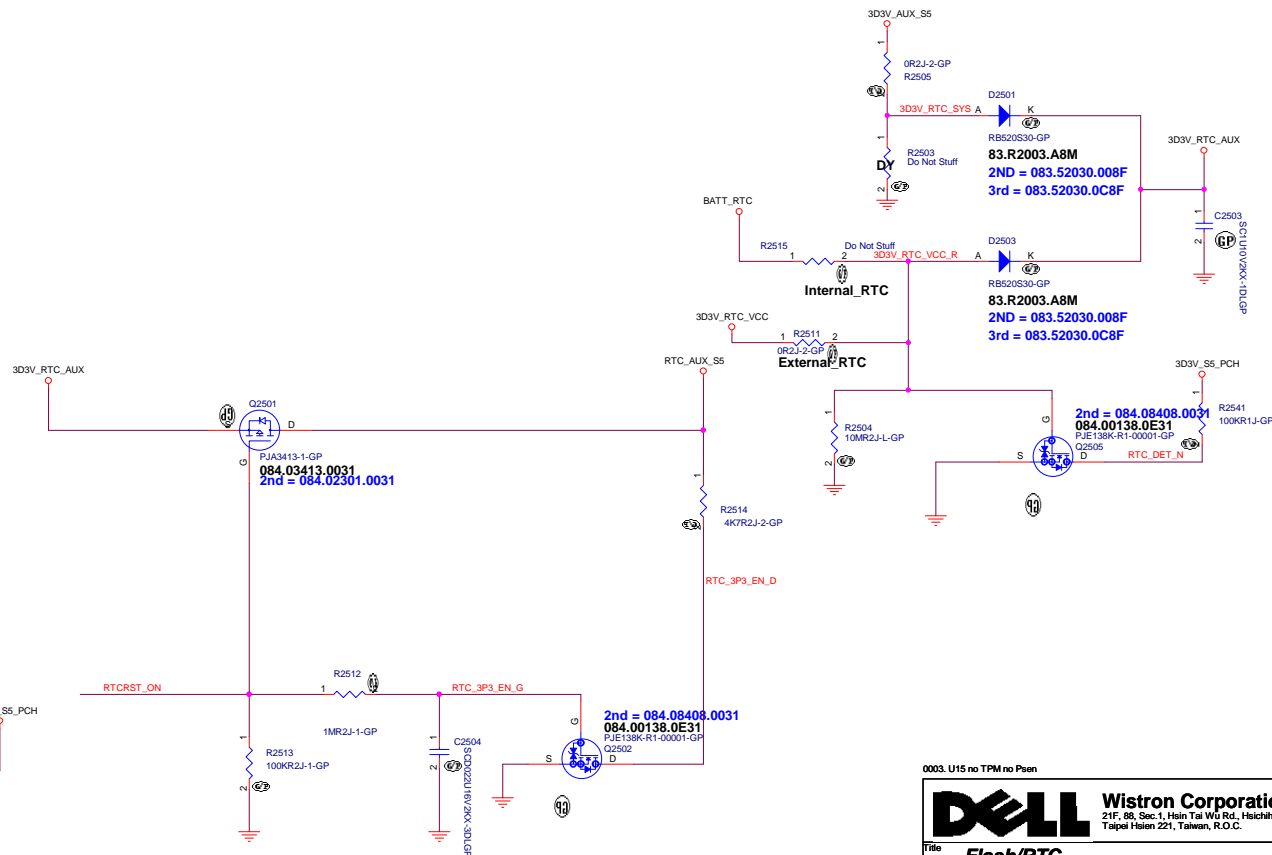
072.25256.0B03

072.25256.0AH1

072.25256.0AG1

32M NON RPMC SOP8

072.25673.0001



0003. U15 no TPM no Psen

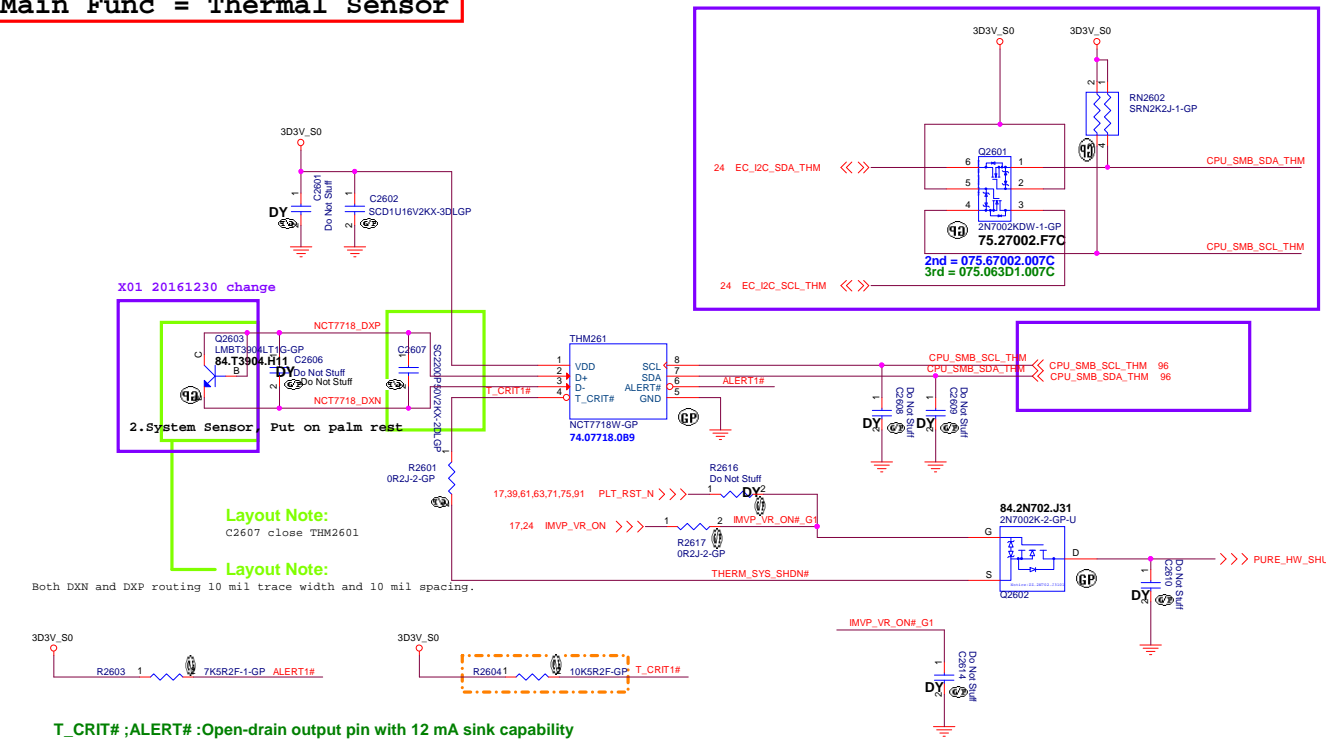
**DELL** Wistron Corporation  
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title <b>Flash/RTC</b>		
Size Custom	Document Number <b>Odin ADL-P</b>	Rev <b>X01</b>
Date: Friday, August 06, 2021	Sheet 25	of 105

https://www.ti.com

R2521.R2524.R2518.R2526.R2520.R2513.R2517.R2515.R2519.R2522	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL

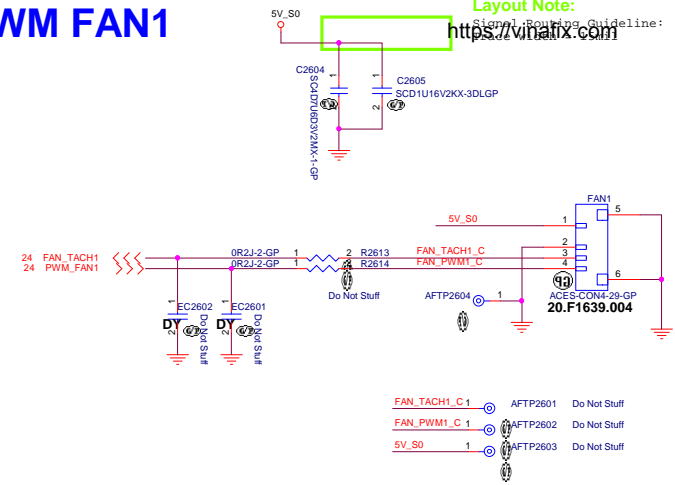
Main Func = Thermal Sensor



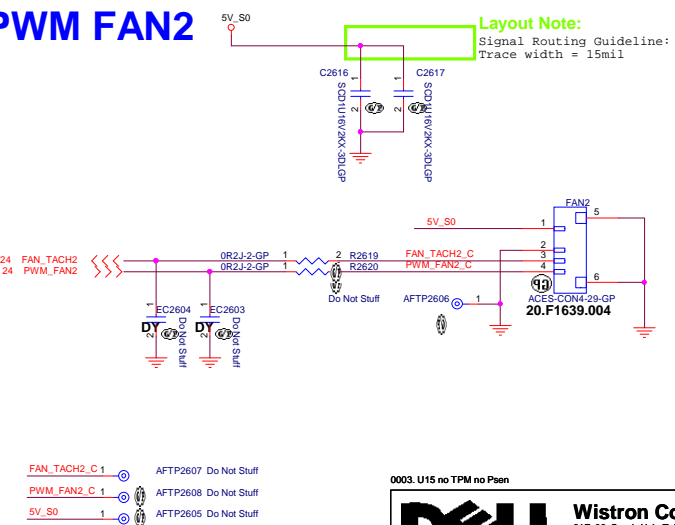
T\_CRIT# ;ALERT# :Open-drain output pin with 12 mA sink capability

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



PWM FAN2



0003. U15 no TPM no Psen

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (Thermal/Fan)**

Size	Document Number	Rev
Custom	<b>Odin ADL-P</b>	<b>X01</b>

Date: Friday, August 06, 2021 Sheet 26 of 105



# Main Func = Audio

## Audio Codec Chip ALC3204

SC2D2U6D3V2MX-DL-GP  
SC2D2U6D3V2MX-DL-GP

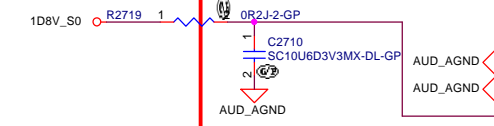
AUD\_HPOUT\_R  
AUD\_HPOUT\_L

https://vinafix.com

19,96 HDA\_SDIN0\_CPU <<<  
19,96 HDA\_SDOUT\_CODEC >>>  
19 HDA\_SYNC\_CODEC >>>  
19 HDA\_BITCLK\_CODEC >>>  
29 AUD\_SPK\_R\_P <<<  
29 AUD\_SPK\_R\_N <<<  
29 AUD\_SPK\_L\_P <<<  
29 AUD\_SPK\_L\_N <<<  
55 DMIC\_SCL\_CODEC <<<  
55 DMIC\_SDA\_CODEC <<<  
66 AUD\_SENSE >>>  
32 NB\_MUTE# >>>  
3,24 SPKR >>>  
24 BEEP >>>  
29,66 AUD\_RING <<<  
29,66 AUD\_SLEEVE <<<  
29 LINE1\_L >>>  
29 LINE1\_R >>>  
29 LINE1\_VREFO <<<  
29 MIC2\_VREFO\_R <<<  
29 AUD\_HPOUT\_L <<<  
29 AUD\_HPOUT\_R <<<

moat  
Analog  
Digital

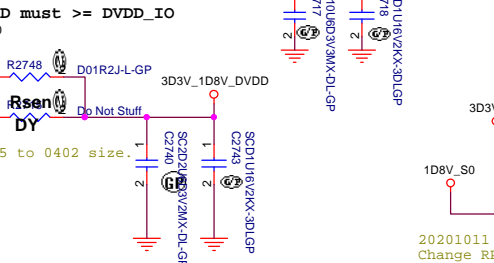
1.8V power rail should be supplied by linear regulator, not switching regulator. If switch regulator is unavailable, please make sure that switch frequency operates at out-band (over 20KHz)



Layout Note:

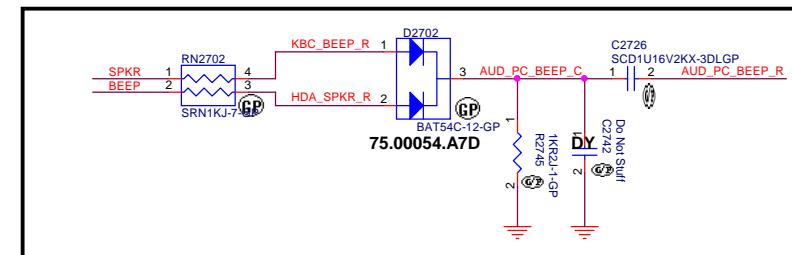
AUD\_SPK\_L\_P  
AUD\_SPK\_L\_N  
AUD\_SPK\_R\_P  
AUD\_SPK\_R\_N

Speaker trace width >40mil @ 2W4ohm speaker power

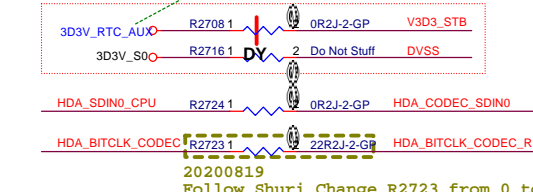


### SIV Auto Test

96 HDA\_BITCLK\_CODEC\_R <<<



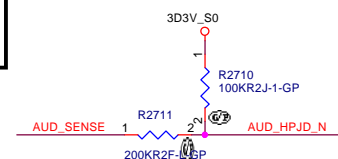
Open drain output. pull up to DVDD or max. 5V  
For RTC Gen9 reset circuit change power rail.  
20170921



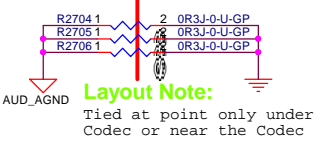
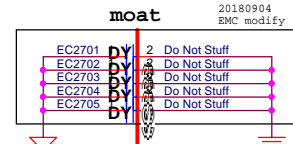
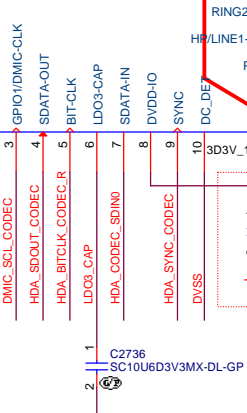
20201011  
Change RP2725 to 0402 size.

place close to pin1  
20200715  
C2720 Change to 0603 Common part

20180911  
Vendor stuff

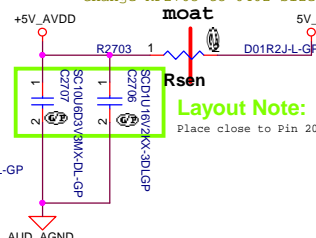


ALC3204  
QFN40 (5X5)  
071.03204.M001



20210504  
Change C2741 & C2739 to 2.2u 6.3V  
Confirmed with vendor.

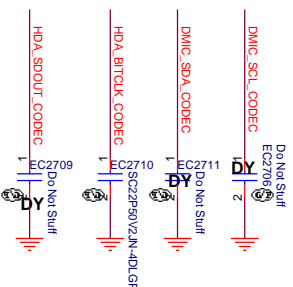
20201011  
Change RP2703 to 0402 size.



Layout Note:  
Place close to Pin 20

Analog  
Digital  
moat

Azalia I/F EMI




20200522  
Vendor suggest:  
1. EC2711 DY that use PCH DMIC.  
2. EC2710, EC2709 should be place nearby PCH  
0003. U15 no TPM no Psen

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio Codec ALC3204		
Size	Document Number	Rev
A3	Odin ADL-P	X01
Date:	Friday, August 06, 2021	Sheet 27 of 105

( Blanking )

0003. U15 no TPM no Psen

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>(Reserved)</b>					
Size	Document Number				Rev
A4	<b>Odin ADL-P</b>				<b>X01</b>
Date: Friday, August 06, 2021			Sheet	28	of 105



Main Func = Audio

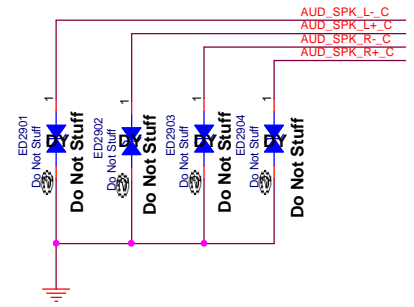
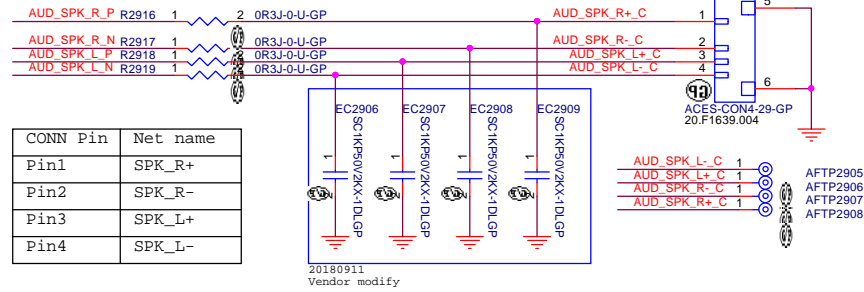
https://vinafix.com

## Speaker

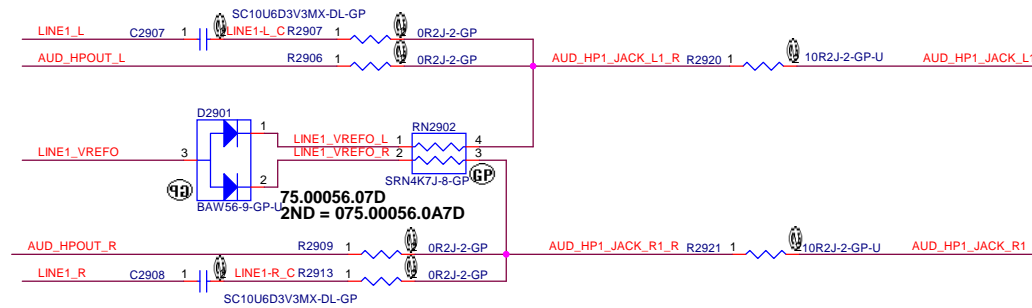
### Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

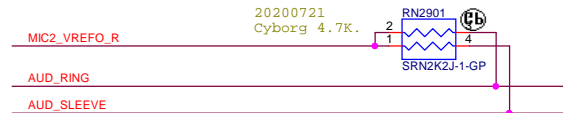
27 AUD\_SPK\_R\_P >>>  
27 AUD\_SPK\_R\_N >>>  
27 AUD\_SPK\_L\_P >>>  
27 AUD\_SPK\_L\_N >>>



27 LINE1\_L >>>  
27 AUD\_HPOUT\_L >>>  
27 LINE1\_VREFO >>>  
27 AUD\_HPOUT\_R >>>  
27 LINE1\_R >>>  
66 AUD\_HP1\_JACK\_L1 >>>  
66 AUD\_HP1\_JACK\_R1 >>>



27 MIC2\_VREFO\_R <<<  
27,66 AUD\_SLEEVE <<<  
27,66 AUD\_RING <<<




0003. U15 no TPM no Psen

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Audio IO</b>			
Size A3	Document Number <b>Odin ADL-P</b>		Rev <b>X01</b>
Date: Friday, August 06, 2021		Sheet 29 of	105

( Blanking )

0003. U15 no TPM no Psen

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)</b>		
Size A4	Document Number <b>Odin ADL-P</b>	Rev <b>X01</b>
Date: Friday, August 06, 2021		Sheet 30 of 105

Main Func = LAN

<https://vinafix.com>

0003. U15 no TPM no Psen

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
LAN RTL8106					
Size	Document Number				Rev
Custom	Odin ADL-P				X01
Date:	Friday, August 06, 2021	1	Sheet	31	of 105

Main Func = LAN

<https://vinafix.com>

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Odin ADL-P**


Date: Friday, August 06, 2021

Rev  
**X01**

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**XFOM&RJ45**

0003, U15 no TPM no Pass



Wistron Corporation  
21F, 88, Sec. 2, Hsin-Tsuen Rd., Hsinchu,  
Taiwan 30501, Taiwan, R.O.C.

Part

Card Reader-RTSS176E

Doc

Odin ADL-P

Rev


201

Order: Friday, August 08, 2025 10:55

Main Func = USB2.0

<https://vinafix.com>

0003, U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Neihu,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

**USB2.0 CONN**


**Odin ADL-P**

**X01**

Date: Friday, August 08, 2021

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0003. U15 no TPM no Psen



Wistron Corporation  
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsinchu,  
Taippei Hsien 221, Taiwan, R.O.C.

Title

USB (REAR IO/ USB3.0 Conn)

Size

Document Number

Custom

Odin ADL-P

Rev

X01

Date

Friday, August 06, 2021

Sheet

35


of

106

SSID = USB Charger

<https://vinafix.com>


0003. U15 no TPM no Psen

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB Charger</b>			
Size	Document Number		Rev
Custom	<b>Cyborg_ICL</b>		<b>X01</b>
Date:	Friday, August 06, 2021	Sheet	36 of 105



(Blanking)

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***USB3.0 PORT***

Size  
A4


Document Number  
***Odin ADL-P***

Rev  
***X01***

Date: Friday, August 06, 2021Sheet 37 of 105

( Blanking )

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

*Reserved*

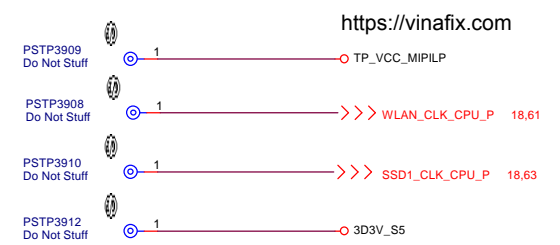
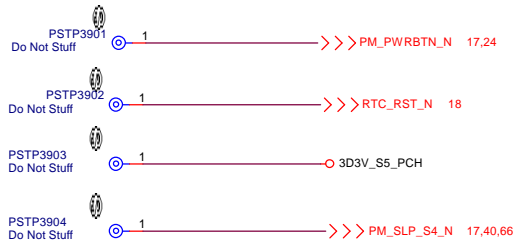
Size  
A4

Document Number  
*Odin ADL-P*

Rev  
*X01*

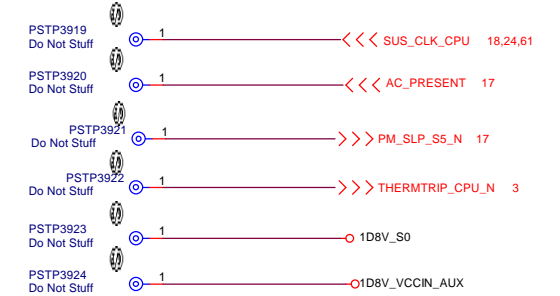
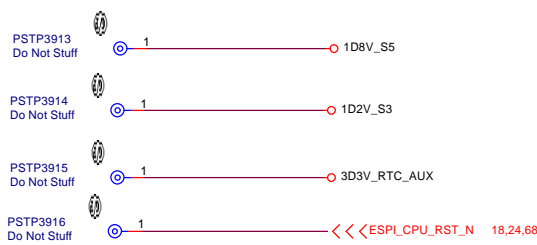
Date: Friday, August 06, 2021Sheet 38 of 105

Place on BOT side



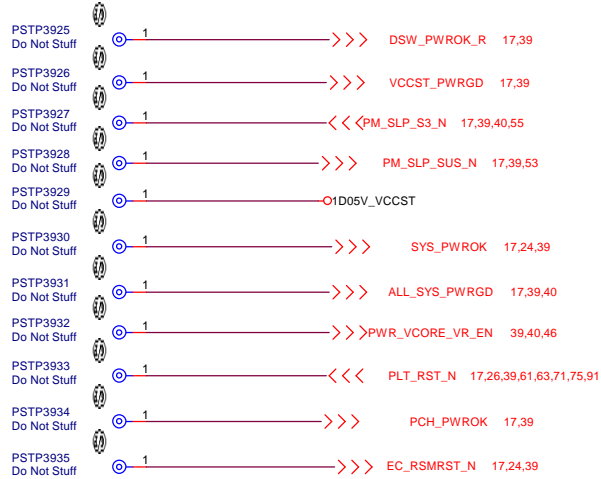
https://vinafix.com

Place on TOP side

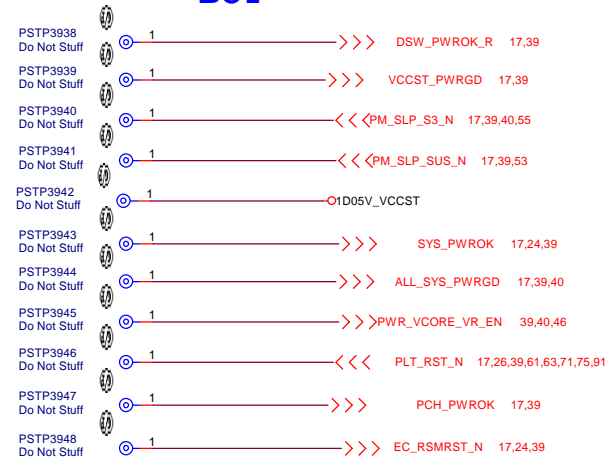


Place on both TOP & BOT side

TOP



BOT



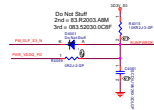
0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
(RSVD)		
Size	Document Number	Rev
A3	<b>Odin ADL-P</b>	<b>X01</b>
Date:	Friday, August 06, 2021	Sheet 39 of 105

## RUNPWROK



## ALL\_SYS\_PWRGD

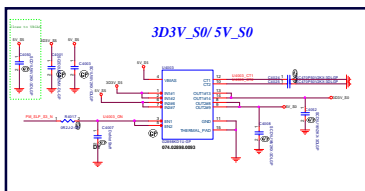
Power-On Reset (POR) Delay Limit



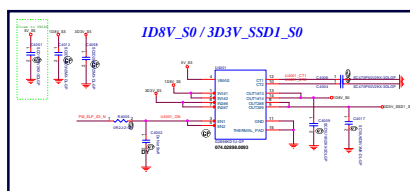
## 3V\_SV\_SS\_EN



## 3D3V\_S0/5V\_S0



## 1D8V\_S0 / 3D3V\_SSD1\_S0



For PWR\_VDDQ\_EN RC delay

Layout Note: Place Close to PDS101

PWR\_VDDQ\_EN

## VCC\_VIP05EXT\_IP05 / VCC\_VNNEXT\_IP05

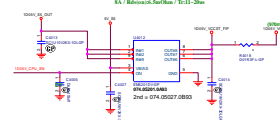
Rev A00 (Rev. 0)

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Intel, the Intel logo, and other marks contained herein are trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

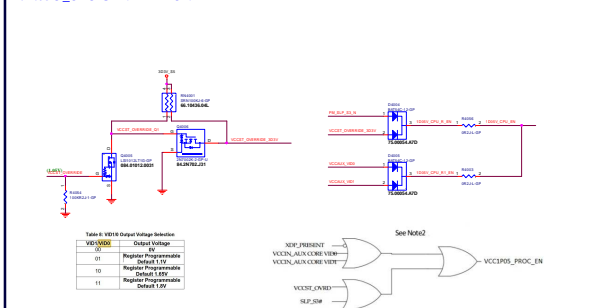
Page 54 of 54 pin reserve bypasses 000.

## 1D05V\_VCCST

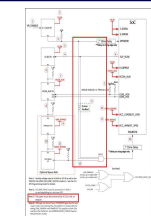
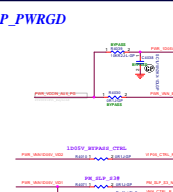


Note 2: VCCIP05\_PROC must be powered on if AUX is on and regulating to a non-zero VDD

## V1.05U\_CPU GENERATION

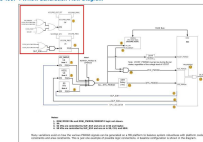


## 1D05V\_BP\_PWRGD




## PWR\_1D8V\_CPU\_EN

Figure 475. PWRGD Generation Flow Diagram



0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Connected\_Standby(1/2)+DS3**

Size  
A4

Document Number  
**Odin ADL-P**


Rev  
**X01**

Date: Friday, August 06, 2021

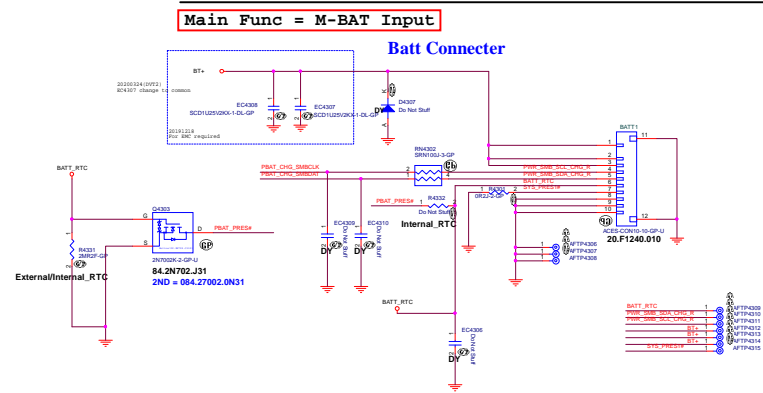
Sheet 41 of 105

( Blanking )

0003. U15 no TPM no Psen

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Connected_Standby(2/2)</b>					
Size A4		Document Number <b>Odin ADL-P</b>			Rev <b>X01</b>
Date: Friday, August 06, 2021		Sheet 42 of		105	

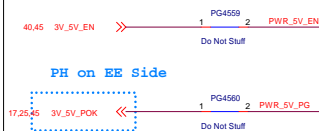
```
56 PWR_SMB_SCL_CHG_R <<>>_____
56 PWR_SMB_SDA_CHG_R <<>>_____
```



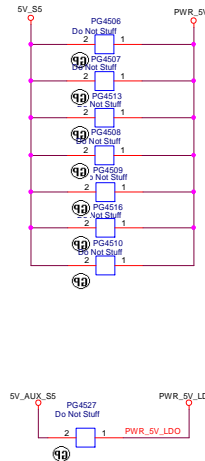




## OFFPAGE-Signal

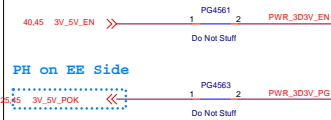
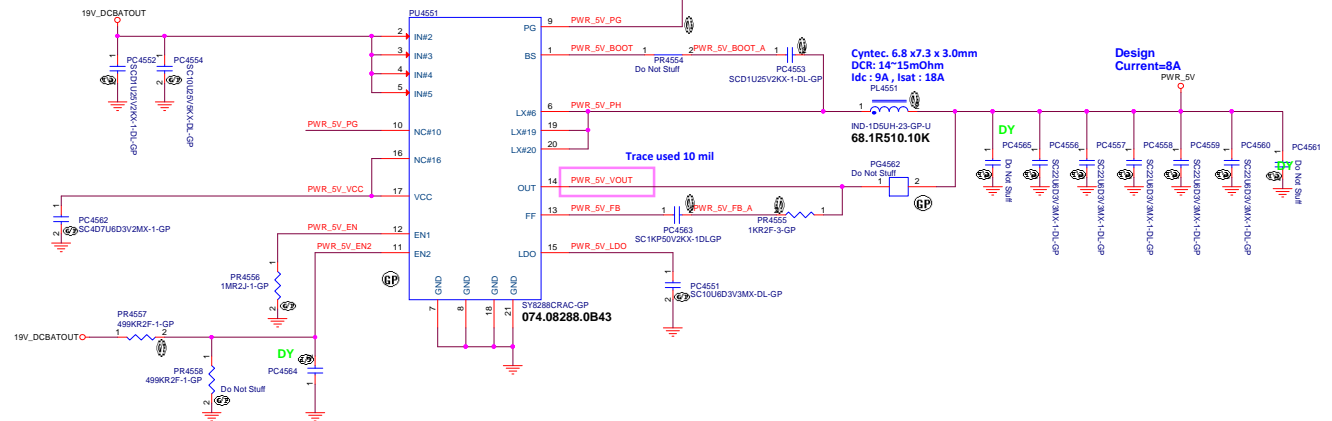
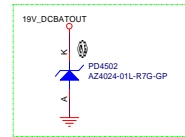


## OFFPAGE-GAP

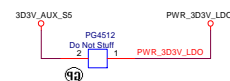


# SY8288C For 5V

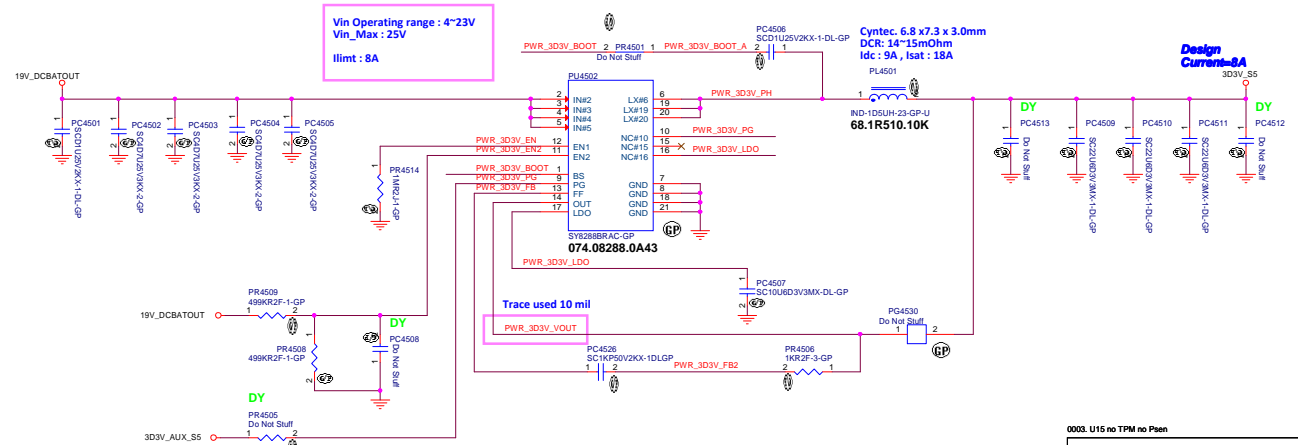
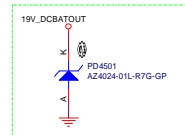
<https://vinafix.com>



## OFFPAGE-GAP

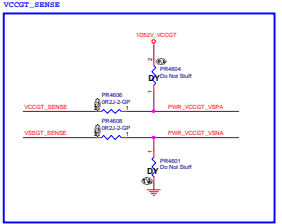
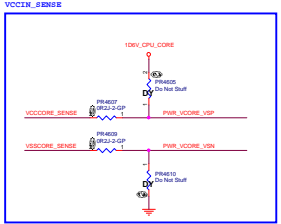
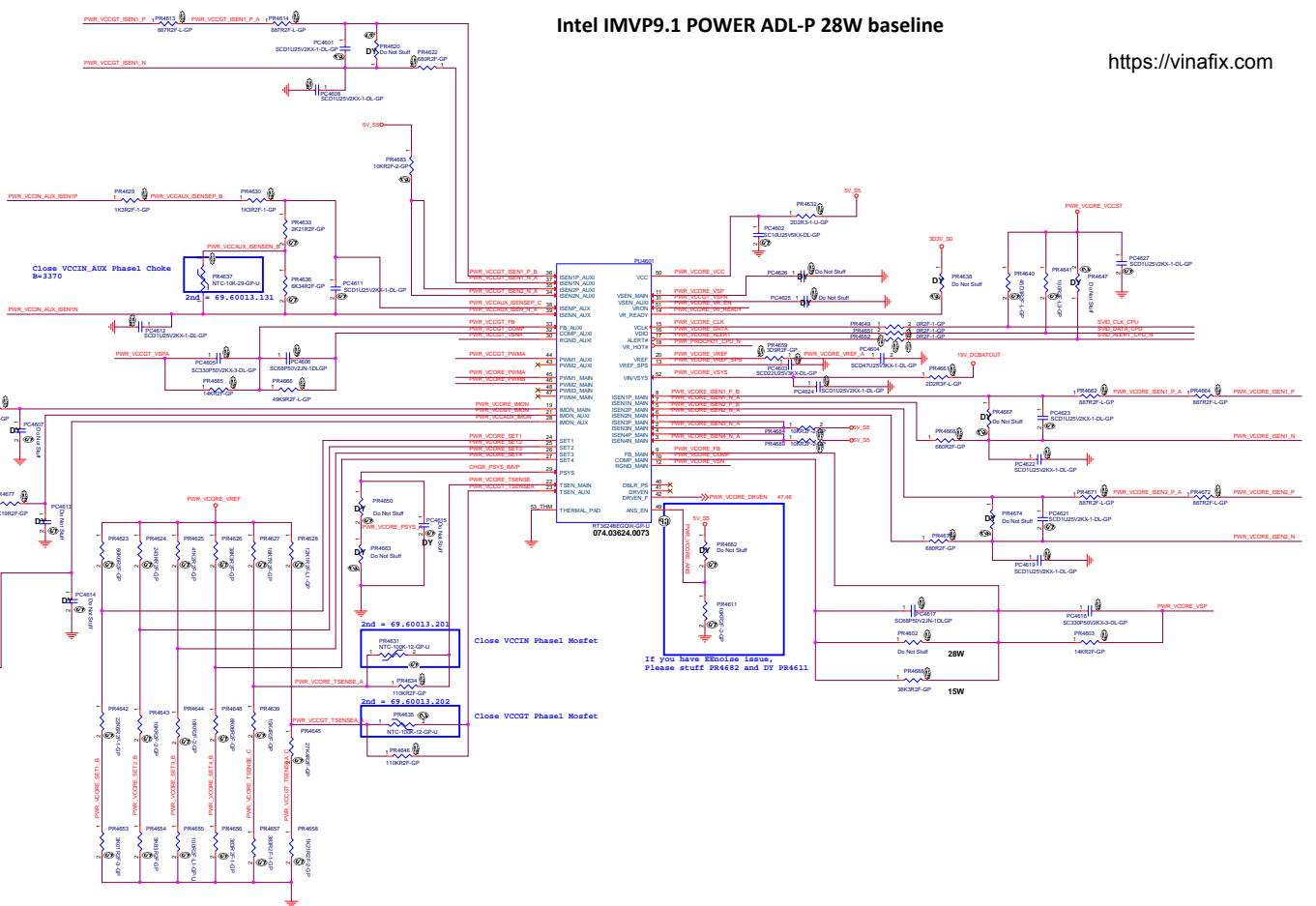


# SY8288B For 3D3V



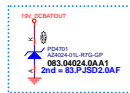
0002\_U15 no TPM no Pisen

<b>DELL</b>		Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		SY8288C & SY8288B_5V/3D3V	
Size	Document Number	Rev	X01
K	Odin ADL-P		
Date: Friday, August 08, 2021	Sheet 45 of 156		

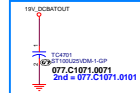


## OFFPAGE

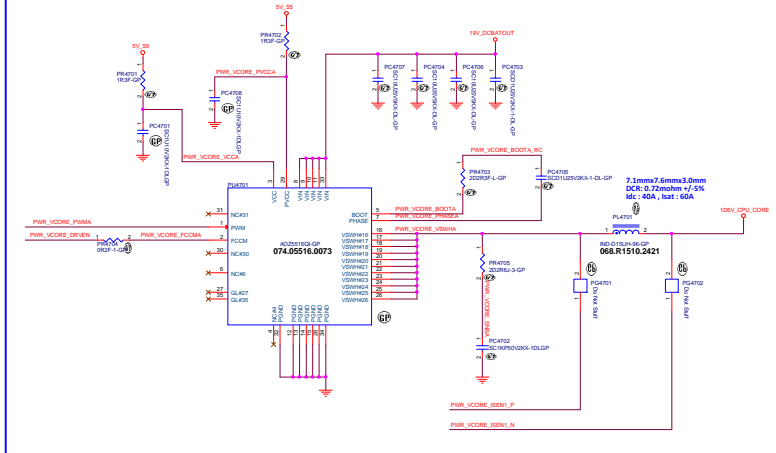
45.48 PWR\_VCORE\_DRV1N >>> \_\_\_\_\_  
 45 PWR\_VCORE\_P1MA >>> \_\_\_\_\_  
 45 PWR\_VCORE\_P1MA >>> \_\_\_\_\_  
 45 PWR\_VCORE\_P1MA >>> \_\_\_\_\_  
 45 PWR\_VCORE\_SEN1\_P <<< \_\_\_\_\_  
 45 PWR\_VCORE\_SEN1\_N <<< \_\_\_\_\_  
 45 PWR\_VCORE\_SEN2\_P <<< \_\_\_\_\_  
 45 PWR\_VCORE\_SEN2\_N <<< \_\_\_\_\_



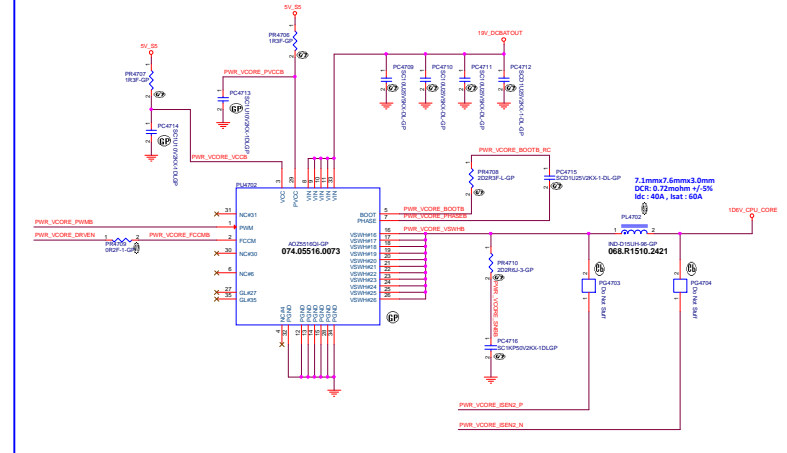
For acoustic noise

<https://vinafix.com>

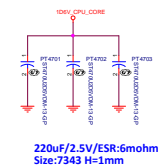
## PHASE1



## PHASE2



## VCCIN Output cap



ADL-P U28 baseline  
 TDC:47A  
 Iccmax:80A  
 96A<OCP>112A

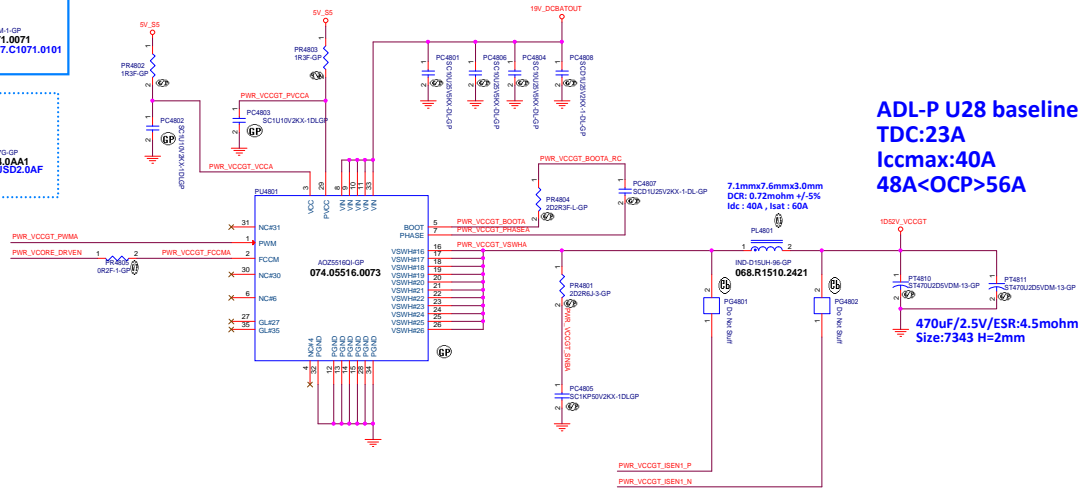
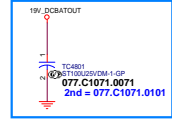
ADL-P U15 baseline  
 TDC:32A  
 Iccmax:60A  
 72A<OCP>84A

Main Func = VCCGT

OFFPAGE

46.47 PWR\_VCORE\_DRIVEN >>>  
46 PWR\_VCCGT\_PWM >>>  
46 PWR\_VCCGT\_IBEN1\_P <<<  
46 PWR\_VCCGT\_IBEN1\_N <<<

For acoustic noise




ADL-P U28 baseline  
TDC:23A  
Iccmax:40A  
48A<OCP>56A

<https://vinafix.com>

15W base-->2+1+1  
15W per-->2+1+1  
28W base-->2+1+1  
28W per-->3+2+1  
45W base-->3+2+1  
45W per-->4+2+1

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

(RSVD)

Size  
A

Document Number  
**Odin ADL-P**

Rev  
**X01**

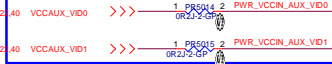
Date: Friday, August 06, 2021

Sheet 49 of 105

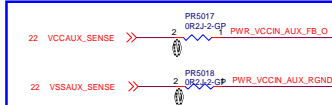
Main Func = VCCIN\_AUX

## OFFPAGE

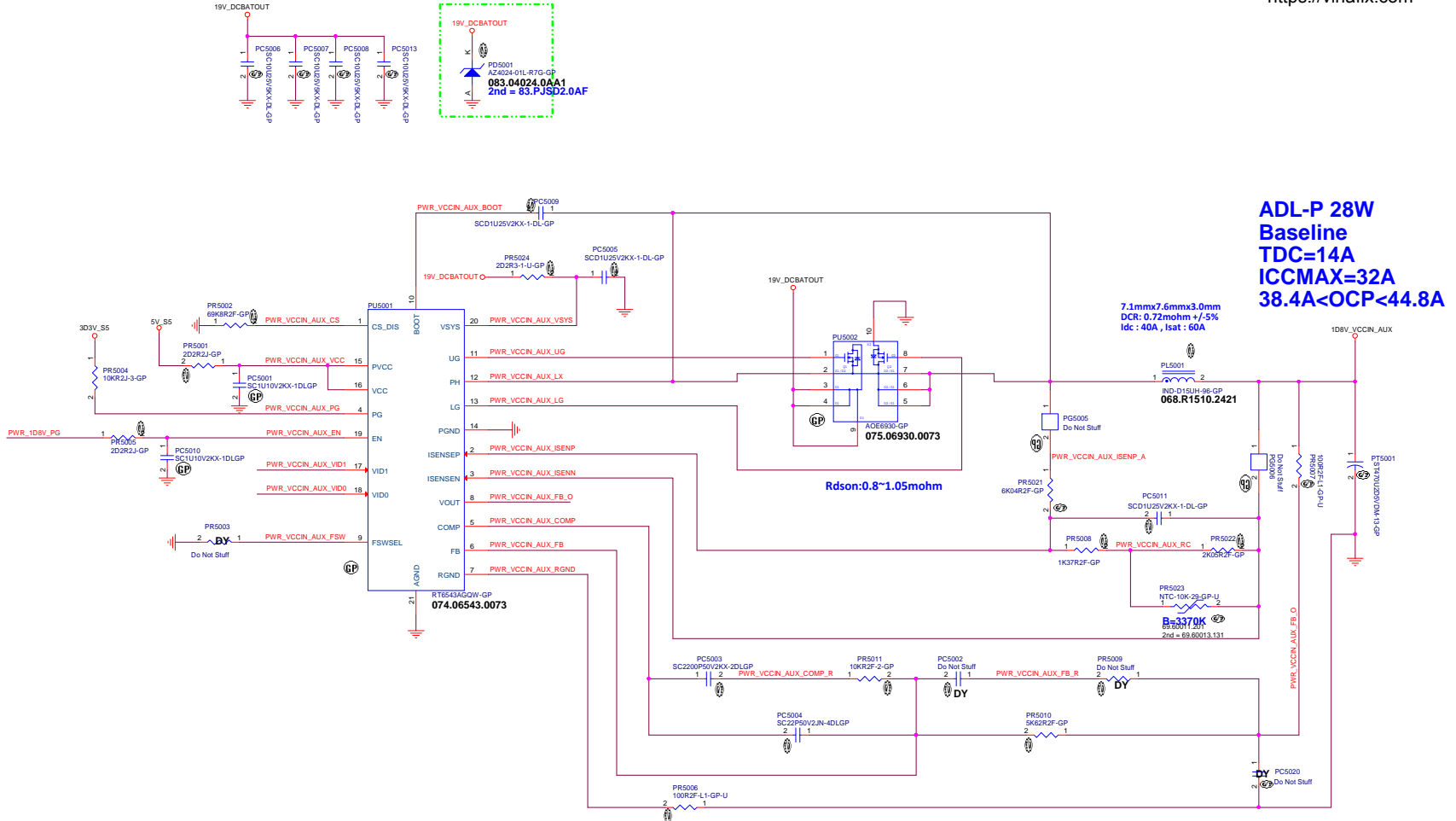
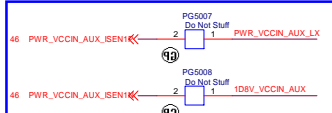
**VID**



## VCCIN\_AUX SENSE



**VCCIN\_AUX ISEN**



0003. U15 no TPM no Psen



Title			
<b>RT6543A VCCIN AUX</b>			
Size A2	Document Number		Rev <b>X01</b>
Date:	Monday, August 05, 2021	Sheet 50 of	105

## OFFPAGE

S5(PM\_SLP\_S4#)

40 PWR\_VDD\_EN >> PWR\_VDD\_EN

S5(PM\_SLP\_S4#)

40 VDDQ\_EN >> VDDQ\_EN

PH on EE Side

40 PWR\_VDDQ\_PG << PWR\_VDDQ\_PG

## OFFPAGE\_GAP

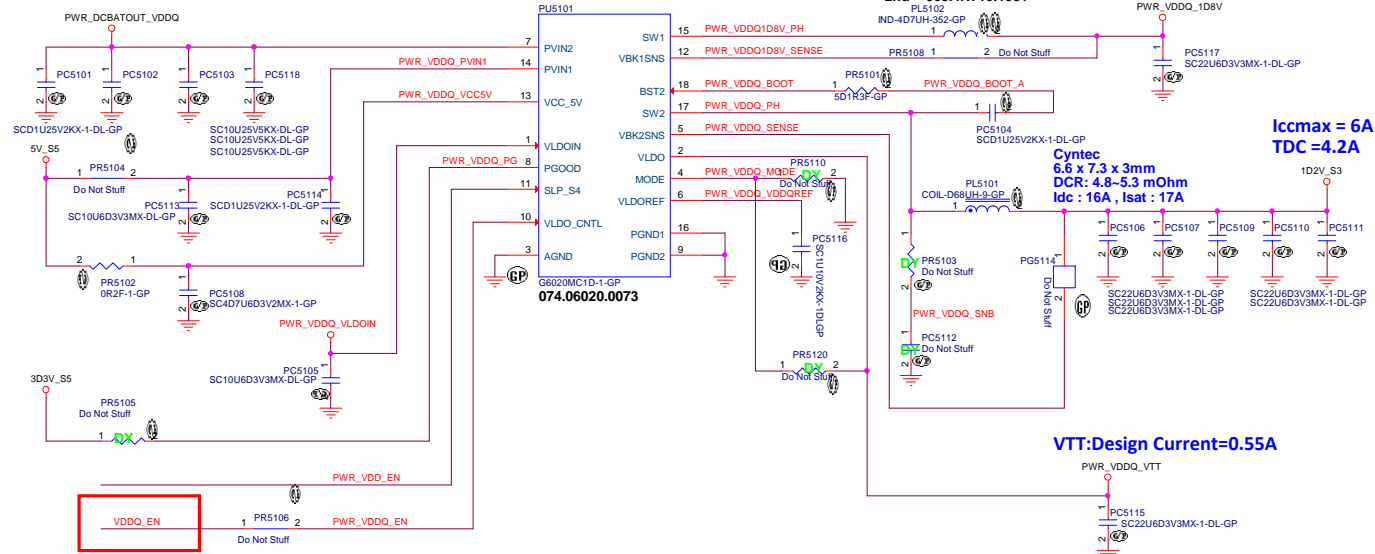
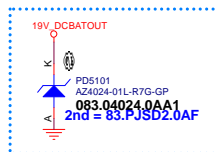
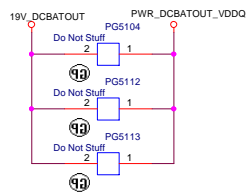
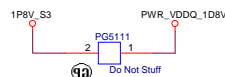
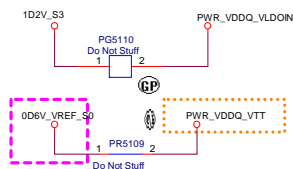


Table 2. Mode Select Different Rails

Mode	Resistor to GND	VBK1 Type	VBK1	VBK2	VLDO
1	0	Buck	2.5V	1.2V	(1/2)*VBK2
2	100kΩ	LDO			
3	200kΩ	Buck	1.8V	1.115V	0.6V
4	High-Z	Buck	1.8V	1.065V	0.5V

setting



# G6020M For LPDDR5

TOKO. 2.5mmx2.0mmX1.2mm  
DCR: 240m Ohm  
Idc: 1.3A, Isat: 1.5A  
2nd = 068.4R710.1981

VDDQ:Design Current=0.35A

Iccmax = 6A  
TDC = 4.2A

Cyntec  
6.6 x 7.3 x 3mm  
DCR: 4.8-5.3 mOhm  
Idc: 16A, Isat: 17A

VTT:Design Current=0.55A

0003. U15 no TPM no Pisen

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (G6020M\_VDDQVTT)**  
Size: Custom  
Document Number: **Odin ADL-P**  
Date: Monday, August 09, 2021  
Rev: **X01**  
Sheet: 51 of 105

SSID = PWR.Plane.Regulator\_1D0V

<https://vinafix.com>

0003. U15 no TPM no Psen



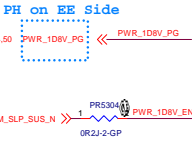
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>POWER (AOZ2262Q_1D0V)</b>	
Size	Document Number		Rev	
A3	<b>Odin ADL-P</b>		<b>X01</b>	
Date: Friday, August 06, 2021		Sheet	52	of 105



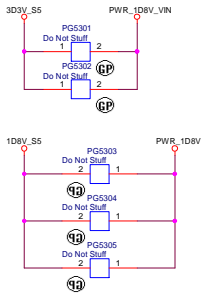
Main Func = 1D8V

OFFPAGE



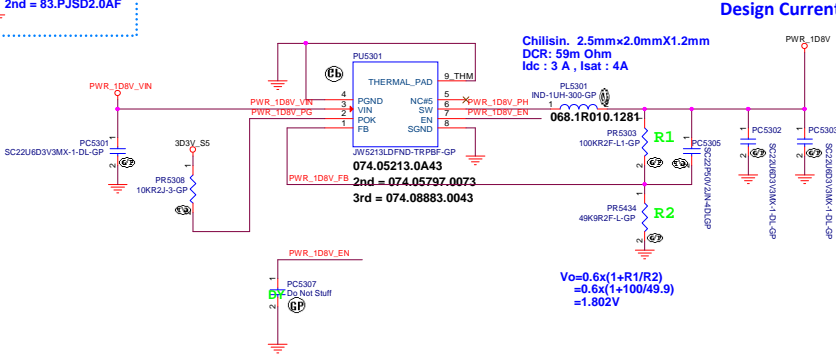
OFFPAGE\_GAP

OFFPAGE\_GAP



SY8883 for 1D8V

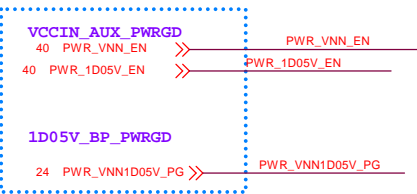
<https://vinafix.com>



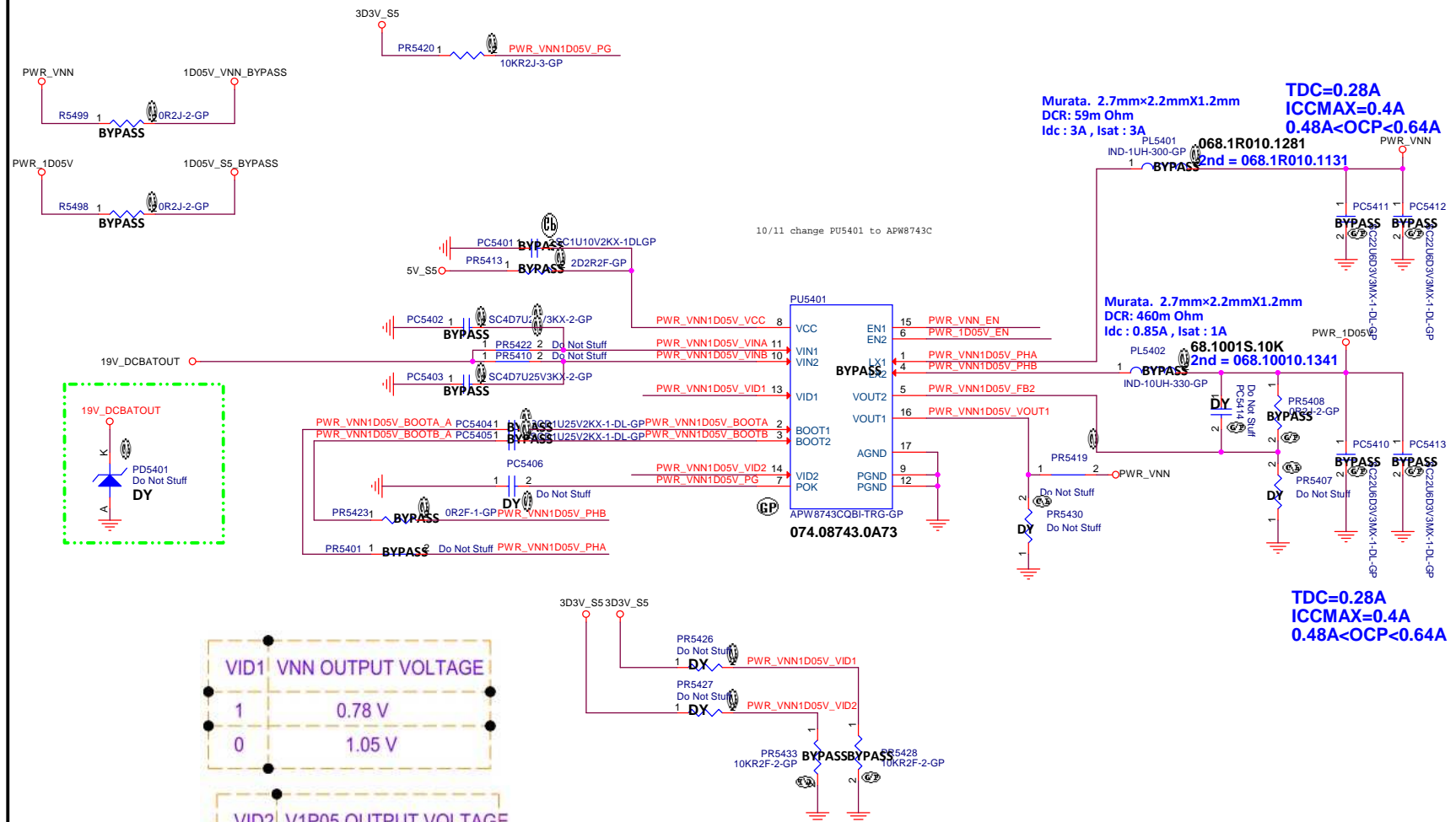
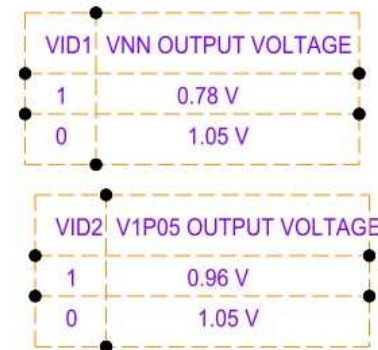
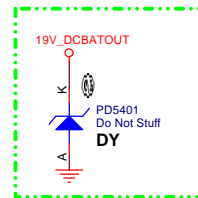
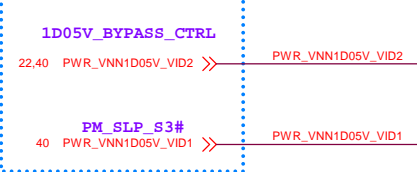
<https://vinafix.com>

## OFFPAGE-GAP

## PH on EE Side



## PH on EE Side

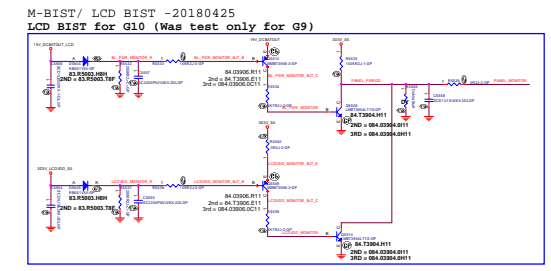


0003. U15 no TPM no Psen



<b>DELL</b>						<b>Wistron Corporation</b> 21 F.R.D., No. 1, Hsin-Yuan Rd., Sec. 2, Taipei 100, Taiwan, R.O.C.	
<b>Display (LCD/Scaler)</b>							
Part Number		Odin ADL-P				X91	
PART NUMBER: 9211							

SIV Auto Test



Main Func = CRT

<https://vinafix.com>

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CRT(Reserved)**

Size  
A3

Document Number  
**Odin ADL-P**

Rev  
**X01**

Date: Friday, August 06, 2021

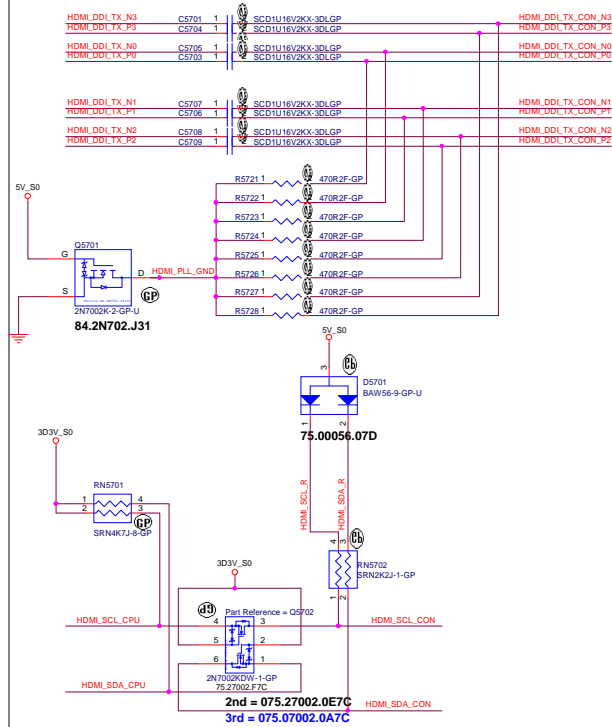
Sheet 56 of 105

# SSID = HDMI Level Shifter/Connector

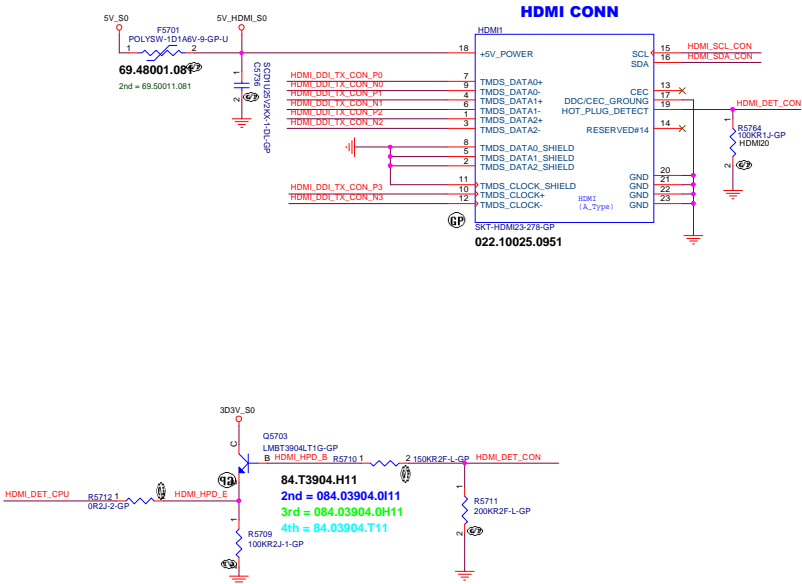
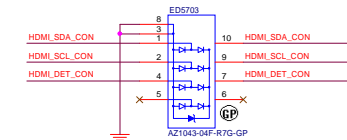
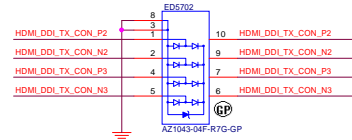
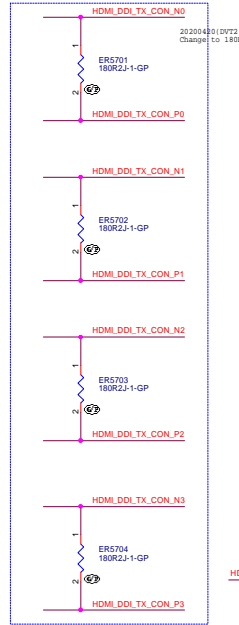
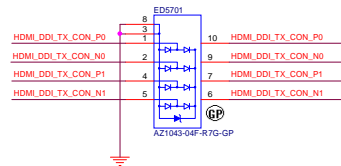
https://vinafix.com

4 HDMI\_DDI\_TX\_N0  
4 HDMI\_DDI\_TX\_P0  
4 HDMI\_DDI\_TX\_N1  
4 HDMI\_DDI\_TX\_P1  
4 HDMI\_DDI\_TX\_N2  
4 HDMI\_DDI\_TX\_P2  
4 HDMI\_DDI\_TX\_N3  
4 HDMI\_DDI\_TX\_P3  
4 HDMI\_DET\_CPU  
4 HDMI\_SCL\_CPU  
4 HDMI\_SDA\_CPU

SIV Auto Test  
96 HDMI\_SCL\_CON  
96 HDMI\_SDA\_CON




EMI Request:



0003\_U15 no TPM no Psen

(Blanking)

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size  
A4

Document Number  
**Odin ADL-P**


Rev  
**X01**

Date: Friday, August 06, 2021

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(Blanking)

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size  
A4

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**Odin ADL-P**

Rev  
**X01**


Date: Friday, August 06, 2021

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Main Func = HDD

<https://vinafix.com>

0003. U15 no TPM no Psen



Wistron Corporation  
21F, 88, Sec.1, Hehai 1st Yulu Rd., Neichia,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

SATA IF HDD/ODD

Size

A2

Document Number

Odin ADL-P

Rev

X01

Date: Friday, August 06, 2021

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**Main Func = WLAN**

```

16 WLAN_PCIE_RX_N <<<
16 WLAN_PCIE_RX_P <<<

16 WLAN_PCIE_TX_N >>>
16 WLAN_PCIE_TX_P >>>

18,39 WLAN_CLK_CPU_P >>>
18 WLAN_CLK_CPU_N <<<
18 WLAN_CLKREQ_CPU_N <<<

```

```

16 BT_USB20_N  <==>
16 BT_USB20_P  <==>

```

17,26,39,63,71,75,91    PLT\_RST\_N>>>\_\_\_\_\_

21	CNV_WR_DN1	<<<	_____
21	CNV_WR_DP1	<<<	_____
21	CNV_WR_DN0	<<<	_____
21	CNV_WR_DP0	<<<	_____
21	CNV_WR_CLKN	<<<	_____
21	CNV_WR_CLKP	<<<	_____
21	CNV_WT_DN1	>>>	_____

21 CNV\_WT\_DN1 >>> \_\_\_\_\_  
21 CNV\_WT\_DP1 >>> \_\_\_\_\_

21 CNV\_WT\_DN0 >>> \_\_\_\_\_  
21 CNV\_WT\_DP0 >>> \_\_\_\_\_

21 CNV\_WT\_CLKN >>> \_\_\_\_\_  
21 CNV\_WT\_CLKP >>> \_\_\_\_\_

```

21  CNV_BRI_RSP_PCH  <<<  _____
15,21 CNV_RGI_DT_PCH  <<<  _____
15,21 CNV_BRI_DT_PCH  <<<  _____
21  CNV_RGI_RSP_PCH  <<<  _____
21  CNV_RF_RST_N     <<<  _____

```

21 CNV\_CLKREQ >>>\_\_\_\_\_

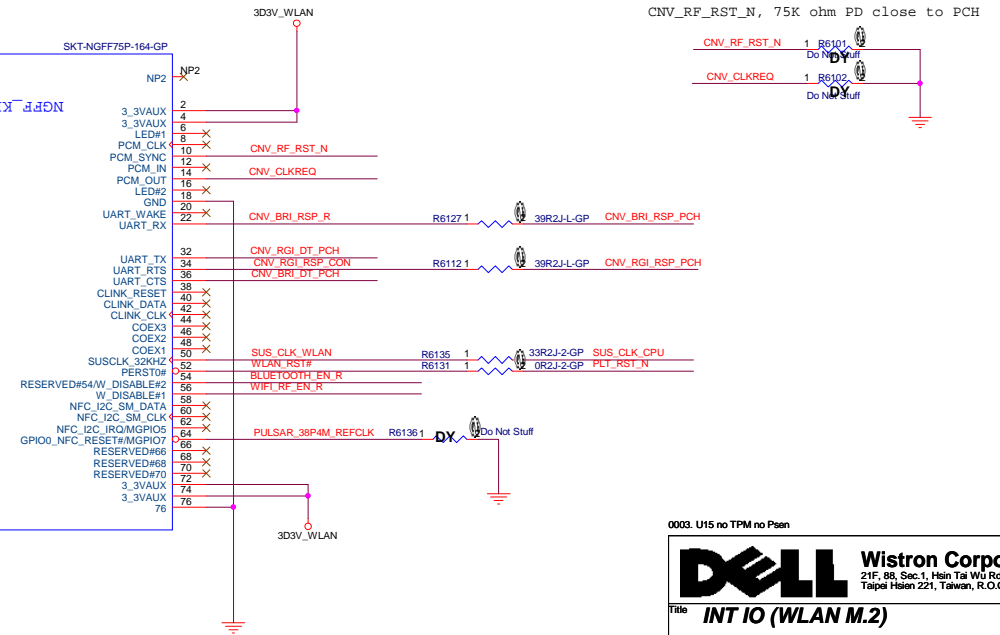
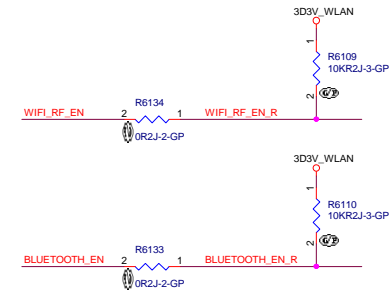
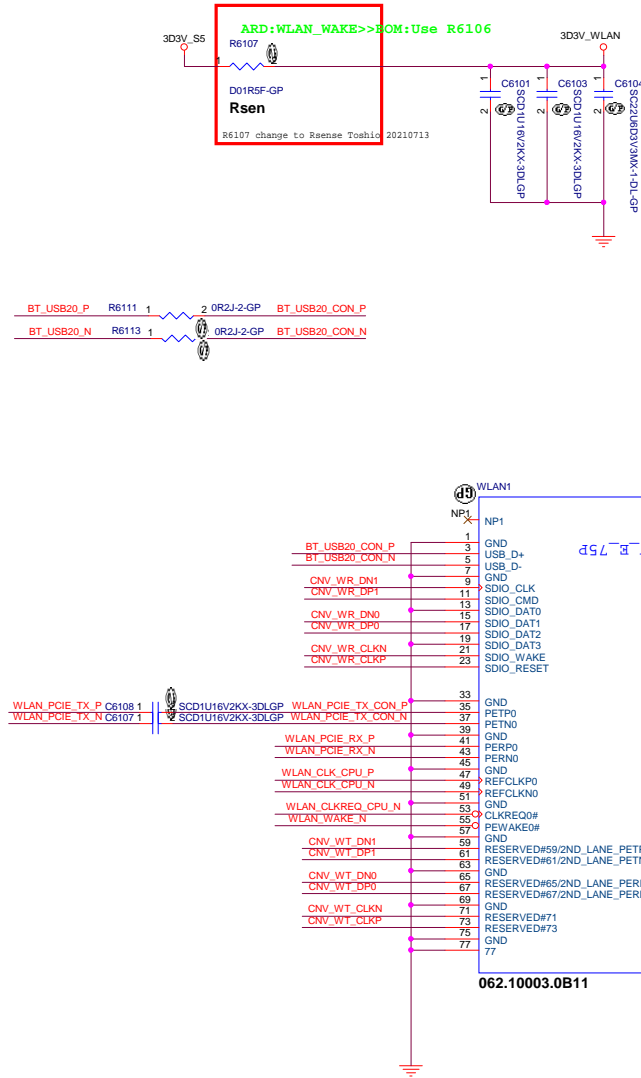
```

19  BLUETOOTH_EN    >>> _____
4   WIFI_RF_EN     >>> _____

18,24,39  SUS_CLK_CPU  >>> _____

```

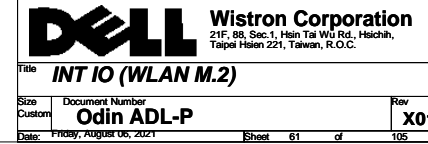
17 WLAN\_WAKE\_N &gt;&gt;&gt; \_\_\_\_\_



<https://vinafix.com>

CNV\_RF\_RST\_N, 75K ohm PD close to PCH

0003. U15 no TPM no Psen



Main Func = WWAN

<https://vinafix.com>

0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN

Size  
A3

Document Number  
**Odin ADL-P**

Date: Friday, August 06, 2021

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**X01**

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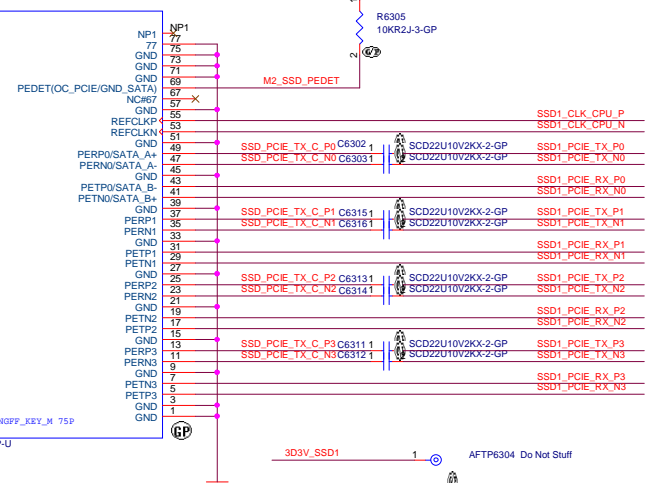
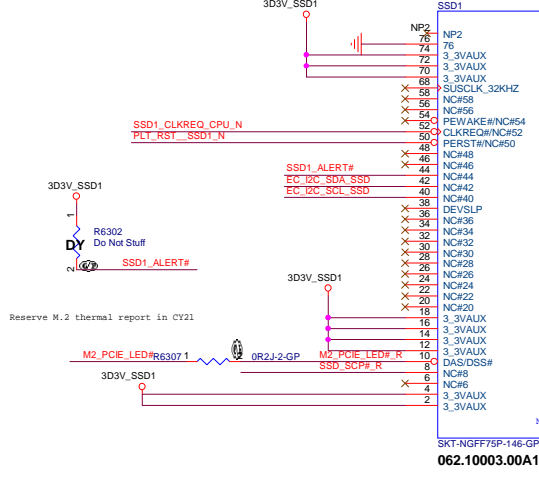
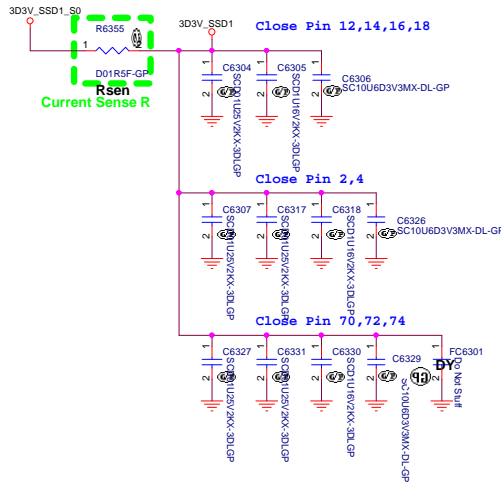
SSID = m-SATA

# Mini Card Connector (NGFF m-SATA)

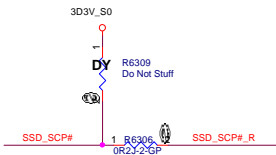
**Important!** SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side, PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

<https://vinafix.com>



SSD1	
18,39	SSD1_CLK_CPU_P
18	SSD1_CLK_CPU_N
18	SSD1_CLKREQ_CPU_N
16	SSD1_PCIE_TX_P0
16	SSD1_PCIE_TX_N0
16	SSD1_PCIE_RX_P0
16	SSD1_PCIE_RX_N0
16	SSD1_PCIE_TX_P1
16	SSD1_PCIE_TX_N1
16	SSD1_PCIE_RX_P1
16	SSD1_PCIE_RX_N1
16	SSD1_PCIE_TX_P2
16	SSD1_PCIE_TX_N2
16	SSD1_PCIE_RX_P2
16	SSD1_PCIE_RX_N2
16	SSD1_PCIE_TX_P3
16	SSD1_PCIE_TX_N3
16	SSD1_PCIE_RX_P3
16	SSD1_PCIE_RX_N3

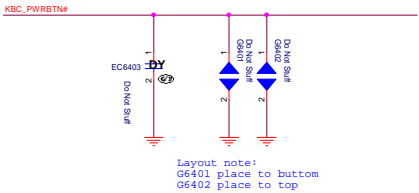


0003. U15 no TPM no Psen

Main Func = Power BTN

24.66 KBC\_PWRBTN# <<< \_\_\_\_\_

Power button



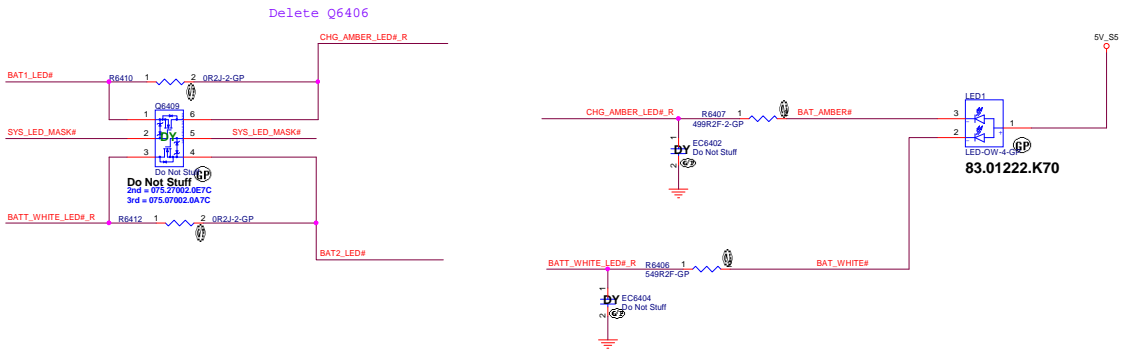
Main Func = Battery LED

Low actived from KBC GPIO

24 BAT1\_LED# >>> \_\_\_\_\_  
24 BAT2\_LED# >>> \_\_\_\_\_  
24.65 SYS\_LED\_MASK# >>> \_\_\_\_\_

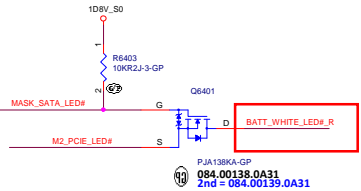
change LED2 to common part & change SCH follow southpeak Toshio 0630

Battery LED1 (AMBER\_LED)



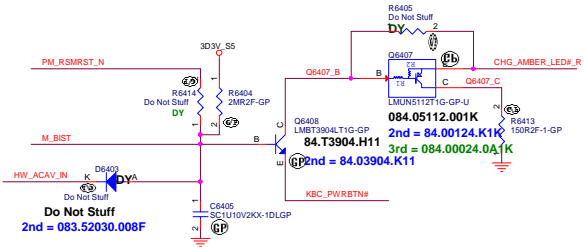
Main Func = HDD LED

24 MASK\_SATA\_LED# >>> \_\_\_\_\_  
63 M2\_PCH\_LED# <<< \_\_\_\_\_



Main Func = M-BIST

17 PM\_RSMRST\_N >>> \_\_\_\_\_  
24 M\_BIST >>> \_\_\_\_\_  
24.44 HW\_ACAV\_IN >>> \_\_\_\_\_



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

0002 U15 no TPM no Pisen

Main Func = KB

24 CAP\_LED#, R >>>

24 F4\_LED#, R >>>

24.64 SYS\_LED\_MASK# >>>

4 KB\_DET# <<<

20 KB\_LED\_BL\_DET# <<<

24 KB\_LED\_PWM >>>

24 KSO00 <<<

24 KSO01 <<<

24 KSO02 <<<

24 KSO03 <<<

24 KSO04 <<<

24 KSO05 <<<

24 KSO06 <<<

24 KSO07 <<<

24 KSO08 <<<

24 KSO09 <<<

24 KSO10 <<<

24 KSO11 <<<

24 KSO12 <<<

24 KSO13 <<<

24 KSO14 <<<

24 KSO15 <<<

24 KSO16 <<<

24 KS00.7 <<<

KSO0

KSO1

KSO2

KSO3

KSO4

KSO5

KSO6

KSO7

KSO8

KSO9

KSO10

KSO11

KSO12

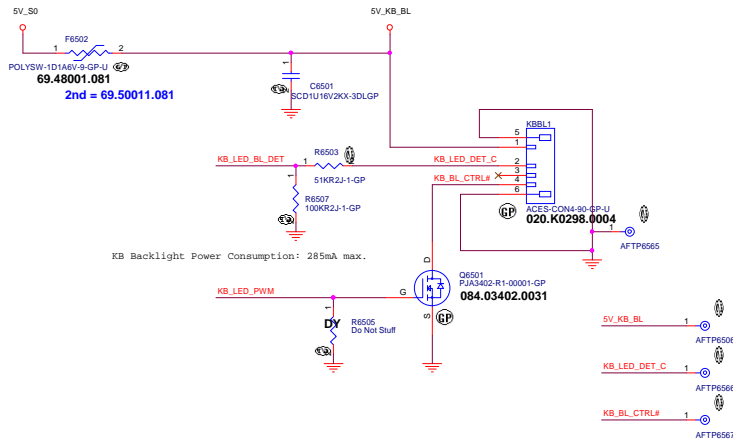
KSO13

KSO14

KSO15

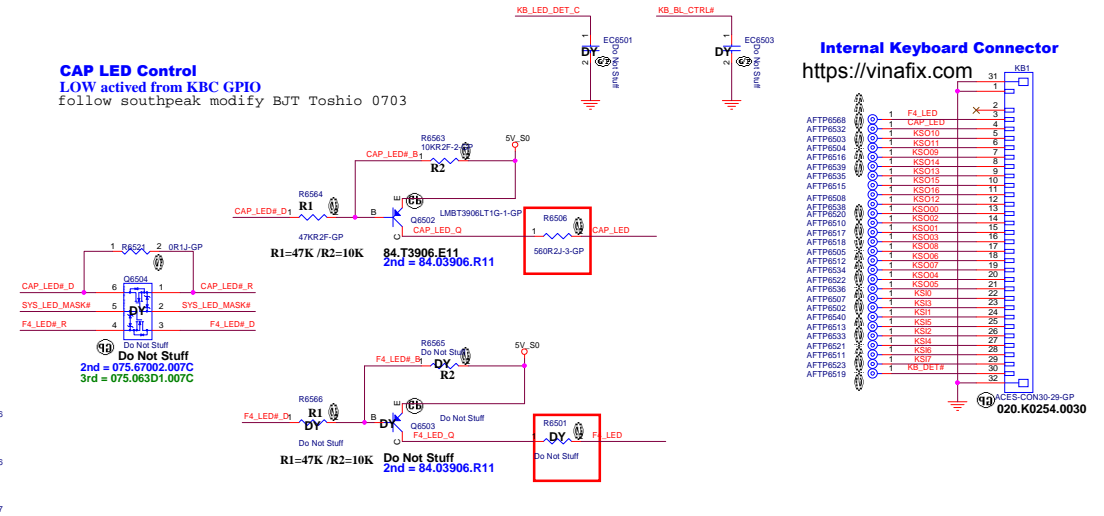
KSO16

**Keyboard Backlight (Reserved)**



**CAP LED Control**  
LOW active from KBC GPIO

LOW active from RBC GFR  
follow southpeak modify BJT Toshio 0703



Main Func = TPAD

## SIV Auto Test

```
96 CPU_I2C_SCL_TP_CON >>-----
```

24,96 EC\_I2C\_SDA\_TP <<<<=====

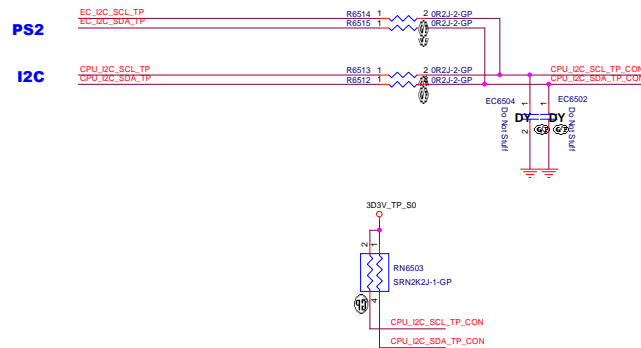
24,96 EC\_I2C\_SCL\_TP <<<<=====

20,96 CPU\_I2C\_SCL\_TP >>>>=====

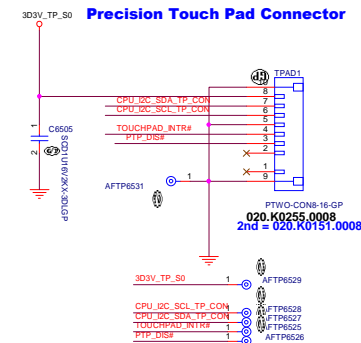
20,96 CPU\_I2C\_SDA\_TP >>>>=====

18,24 TOUCHPAD\_INTR# <<<< \_\_\_\_\_  
24 PTP\_DIS# <<<< \_\_\_\_\_

## Support PTP

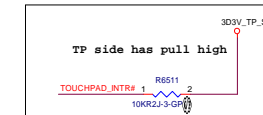


## Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Need to check if it is Active High or Active Low  
and check if there is PH on TPAD side.

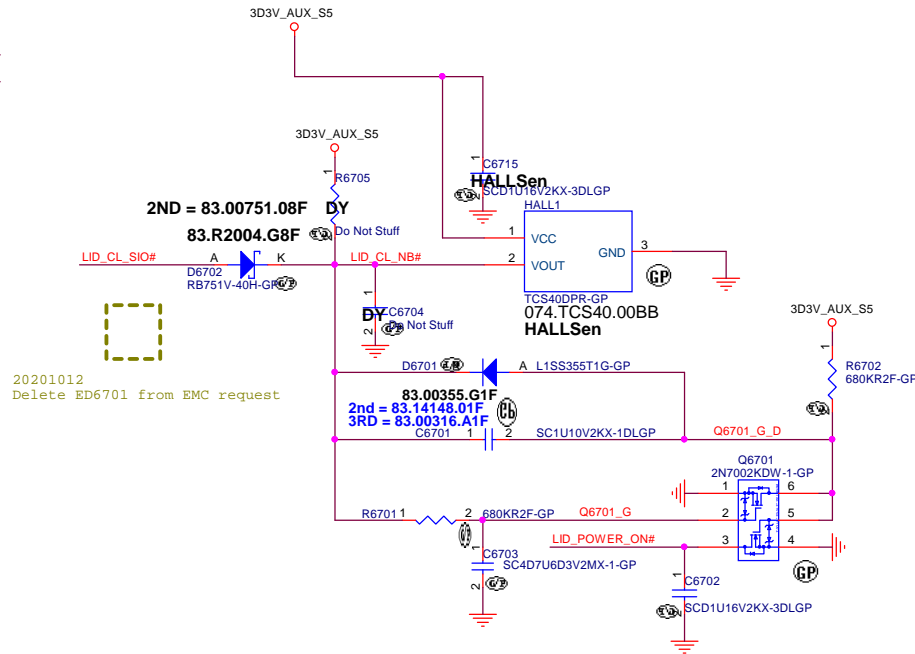




# Main Func = HALL SENSOR

<https://vinafix.com>

20,24,66 LID\_CL\_SIO# <<<—  
24 LID\_POWER\_ON#>>>—



0003. U15 no TPM no Psen



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A3

Document Number

**Odin ADL-P**

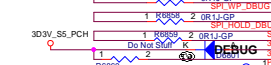
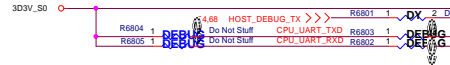
Rev

**X01**

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## 24,64,66 KBC\_PWRBTN# &gt;&gt;&gt;-




0003. U15 no TPM no Psen			
<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Ta Wu Rd., Hsichah, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Debug (LPC debug)</b>			
Size A2	Document Number <b>Odin ADL-P</b>	Rev	<b>X01</b>
Date:	Friday, August 08, 2021	Sheet	68 of 106



( Blanking )

0003. U15 no TPM no Psen

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size	Document Number				Rev
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```

20 GSEN2_INT1_C << >> _____
20 GSEN2_INT2_C << >> _____

20,96 CPU_I2C_SDA_GSENSOR << >> _____
20,96 CPU_I2C_SCL_GSENSOR << >> _____

```

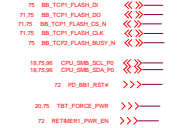
<https://vinafix.com>



Main Func = TBT

HP team on applying, only murata have sample can meet Intel request

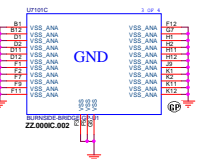
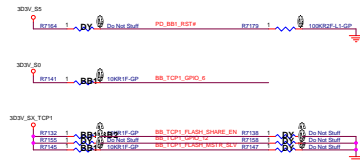
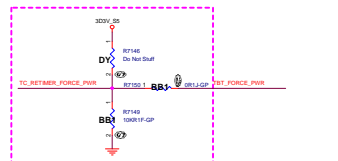
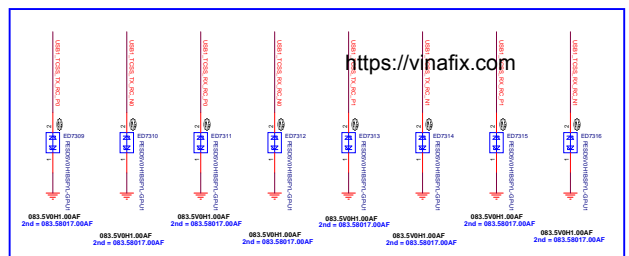
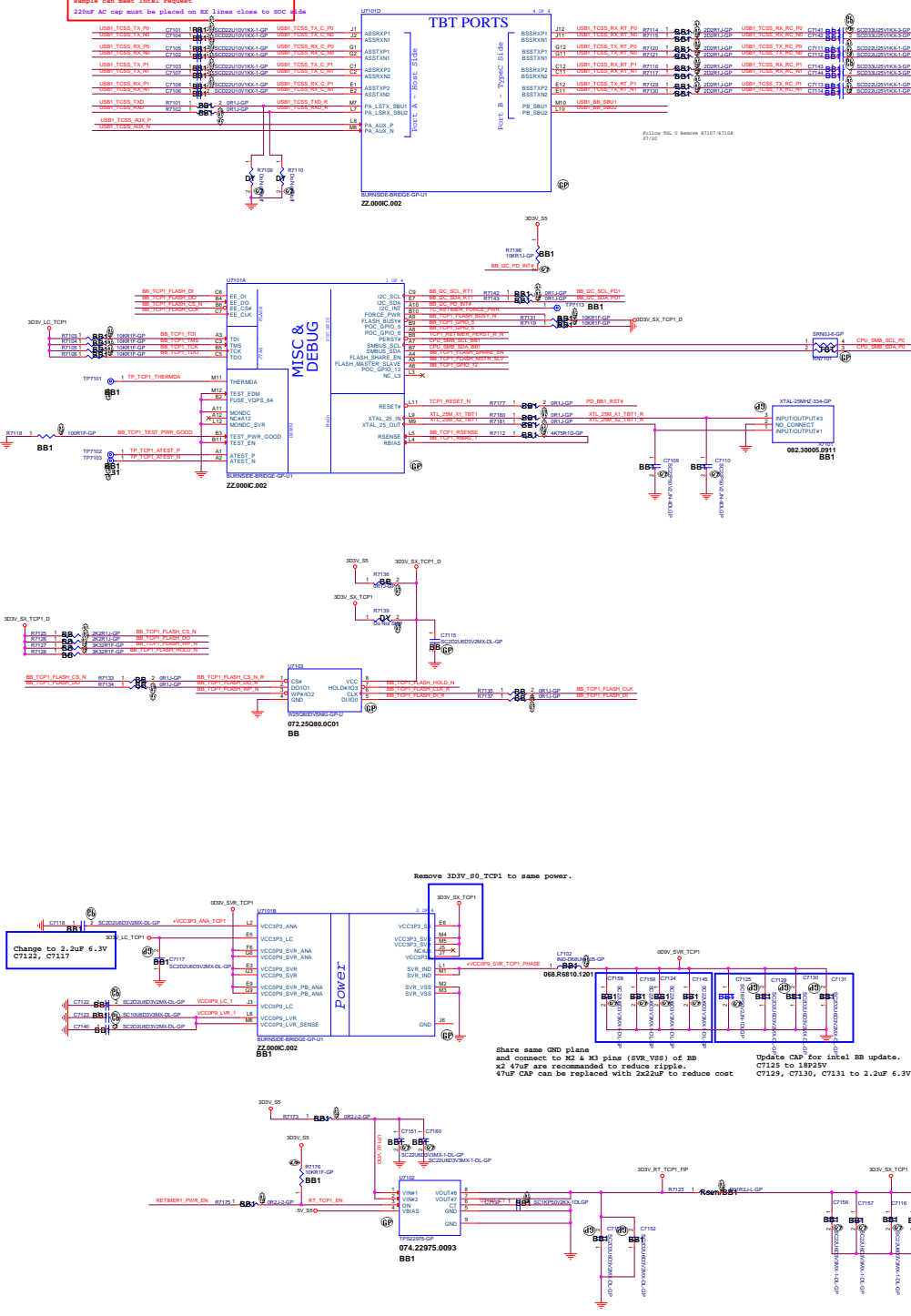
220nF AC cap must be placed on EX lines close to SOC side



PCH to BB

### Type-C PD

### SIV Auto Test



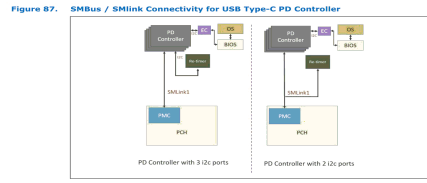
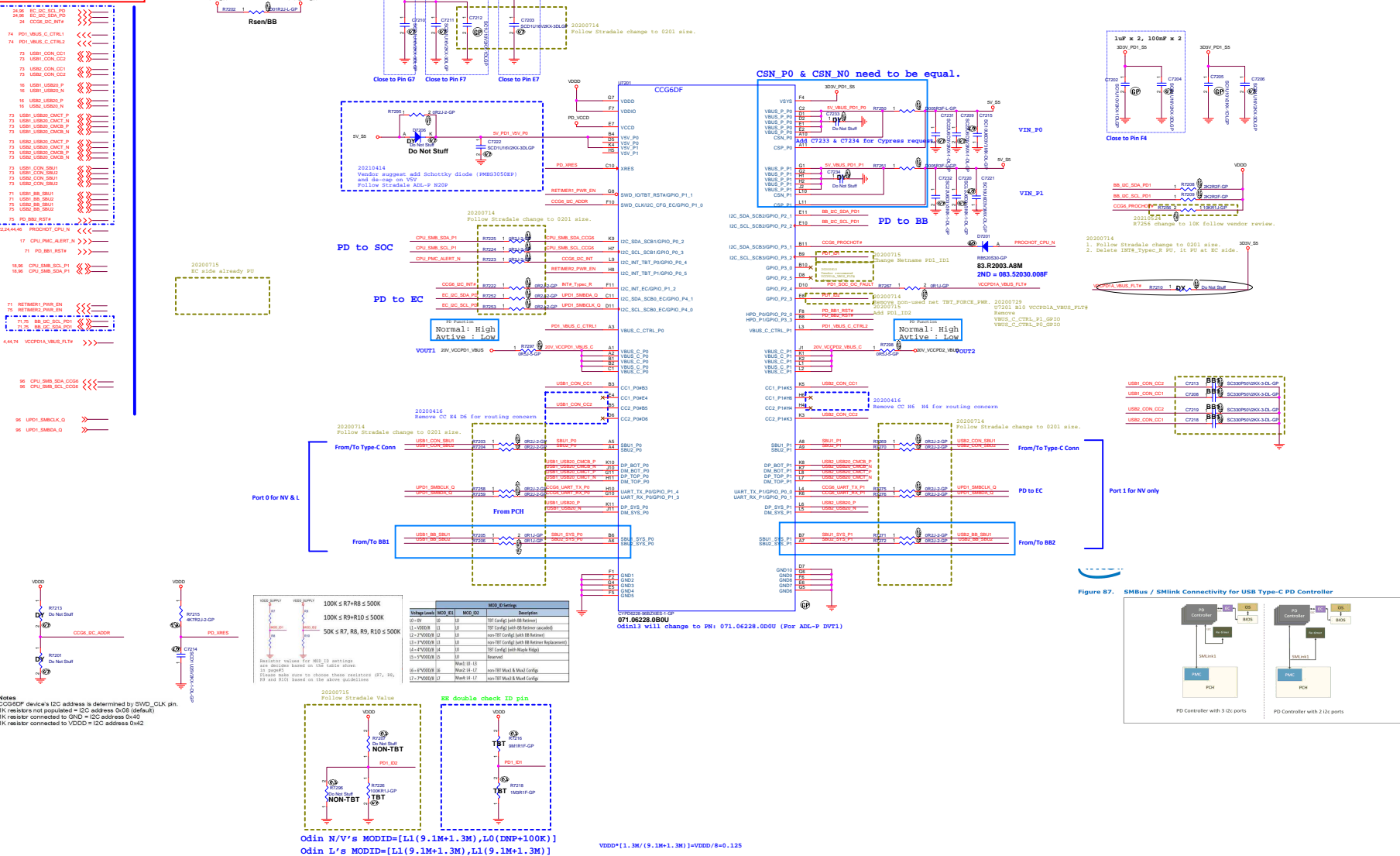
Share same GND plane  
and connect to M2 & M3 pins (SVR\_VSS) of BB  
x2 47uF are recommended to reduce ripple.  
47uF CAP can be replaced with 2x22uF to reduce cost

Update CAP for intel BB update.  
C7125 to 18P25V  
C7129, C7130, C7131 to 2.2uF 6.3V

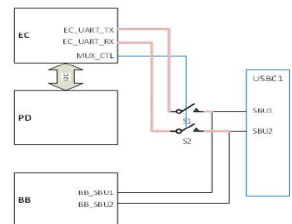
Main Func = TypeC

Follow Hellcat15 Upsell TGL

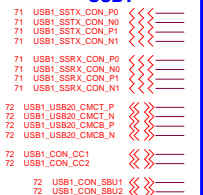
https://vinafix.com



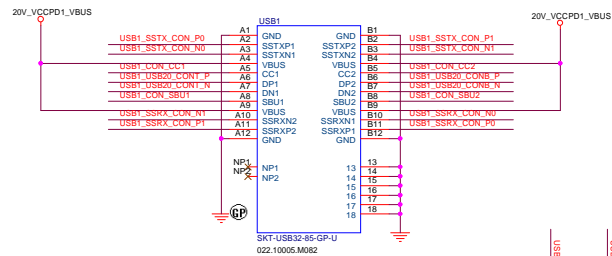
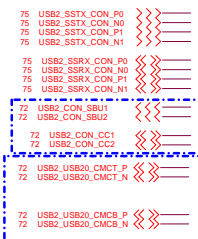
PD_ID1		PD_ID2	
R7216	931MR	R7218	100KR
R7218	1.3MR	R7207	931MR
R7207	100KR	R7226/R7296	1.3MR



## USB1



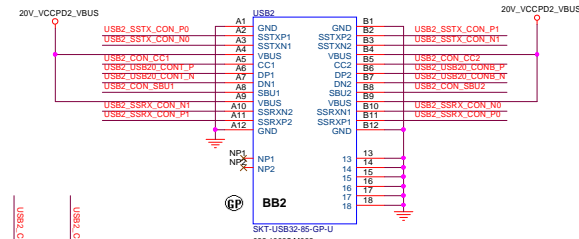
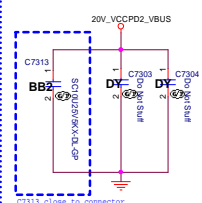
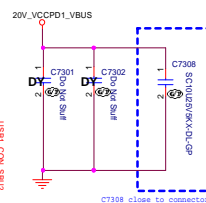
## USB2



BLM6NSN900HY2D-GP  
068.09002.2001  
2nd = 68.02002.061  
3rd = 068.01012.2011



DLM0NSN900HY2D-GP  
068.09002.2001  
2nd = 68.02002.061  
3rd = 68.01012.2011



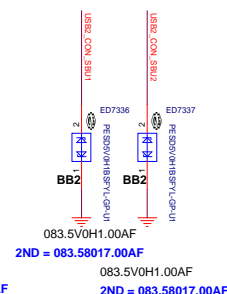
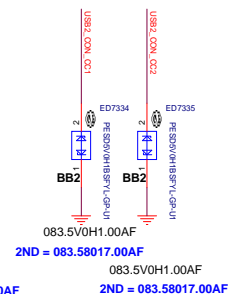
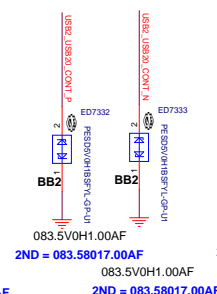
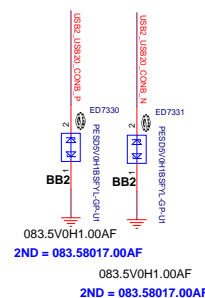
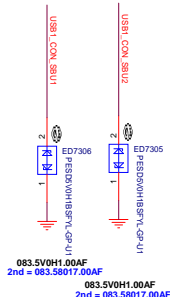
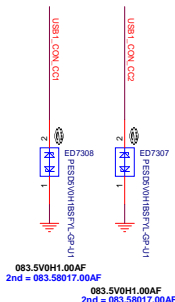
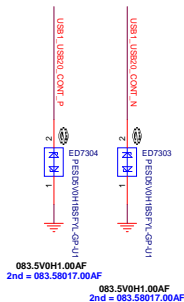
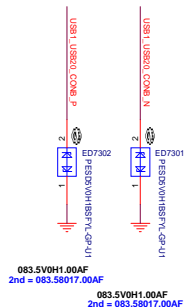
20200821  
Type C connector need change to 022.10005.M082



DLM0NSN900HY2D-GP  
068.09002.2001  
2ND = 68.02002.061



DLM0NSN900HY2D-GP  
068.09002.2001  
2ND = 68.02002.061



0003. U15 no TPM no Psen

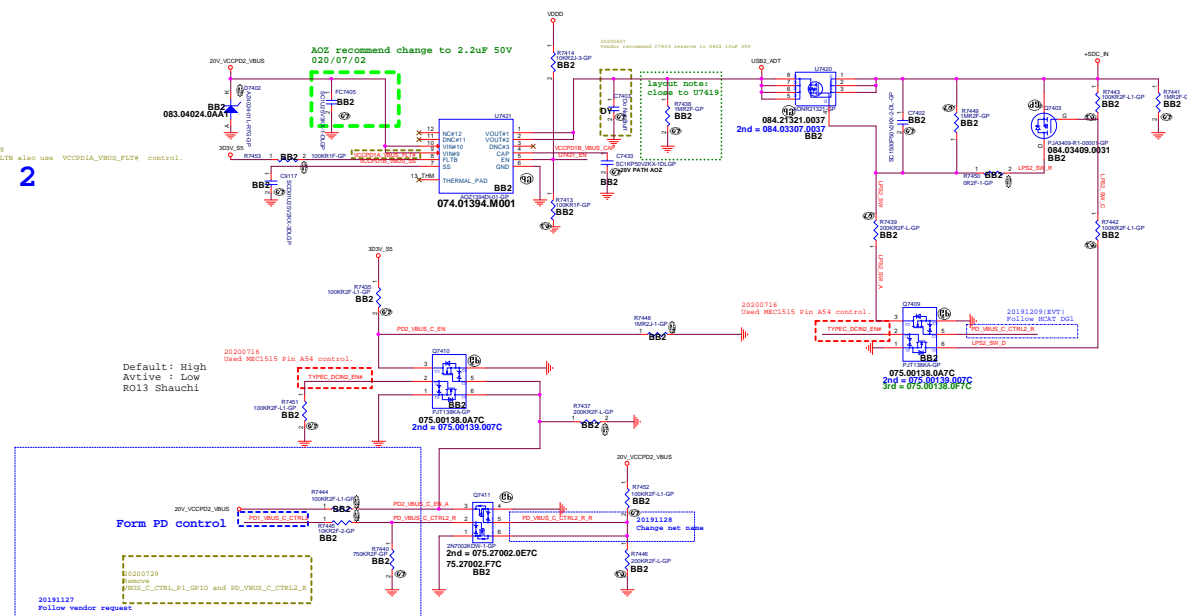
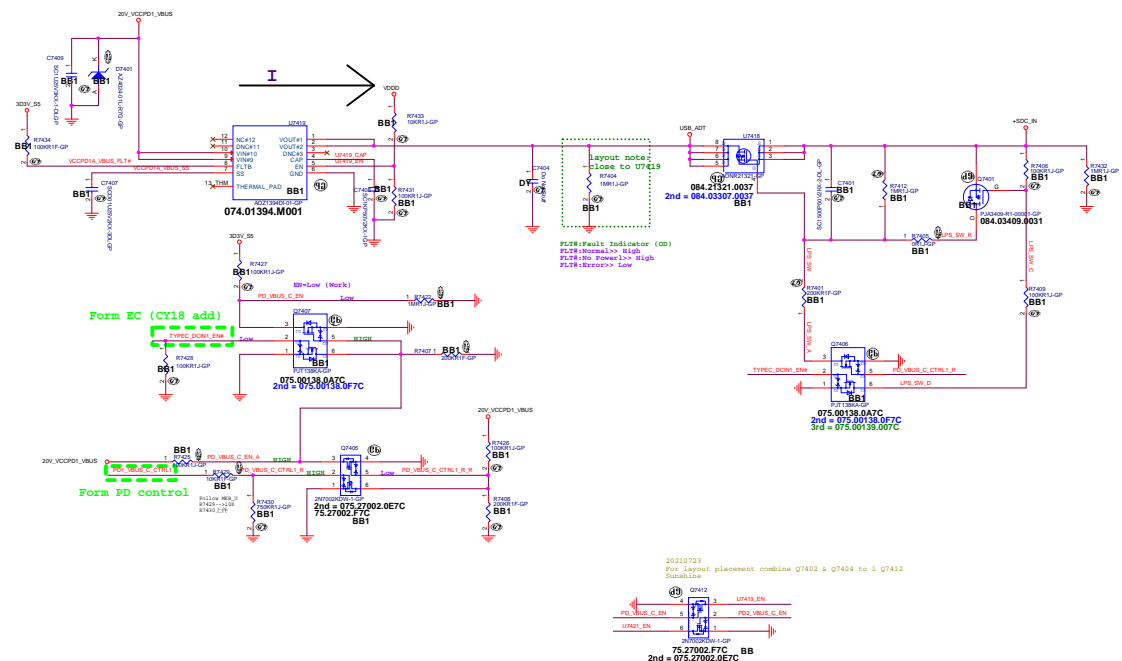


**Title**  
**EXT IO (Thunderbolt(3/3)/Type C Conn)**

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**Main FUNC = LPS**

<https://vinafix.com>



Main Func = TBT

USB2

BB

BB

Type-C PD

SV Auto Test

SV Auto Test

10 team on applying, only murata have sample can meet intel request  
220uF AC cap must be placed on X2 close close to SOC side

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

TBT PORTS

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

MISC & DEBUG

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

BB TO PCH(TBT)

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

Power

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

SV Auto Test

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

SV Auto Test

20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137

RETIMER\_PWR\_EN RTW3 1 082

SV Auto Test

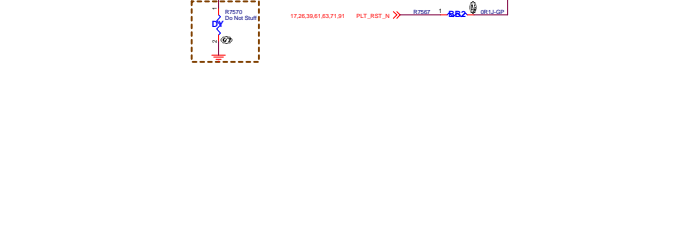
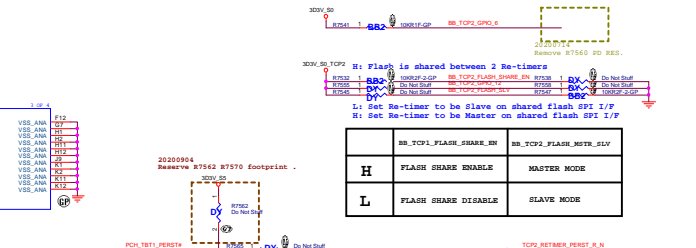
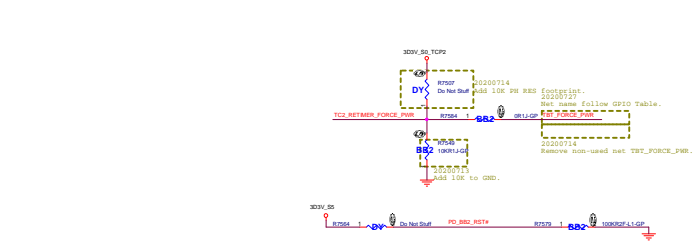
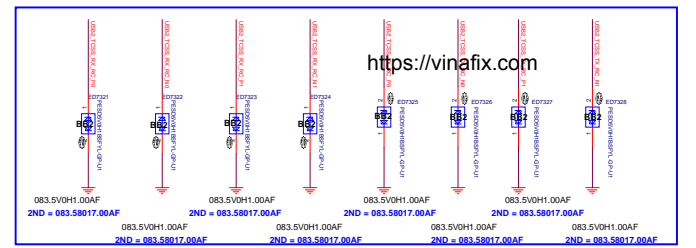
20200713  
Change to G201 Footprint .

20200522  
Delete 00hm Res.

20200713  
Remove U7501 A12 TP.

Change to 2.2uF 6.3V  
C7129, C7137


RETIMER\_PWR\_EN RTW3 1 082



Update CAP for intel BB update.  
C7125 to 18025V  
C7129, C7130, C7131 to 2.2uF 6.3V

Main Func = dGPU

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Title

GPU DIGITALOUT (2/5)

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Main Func = dGPU

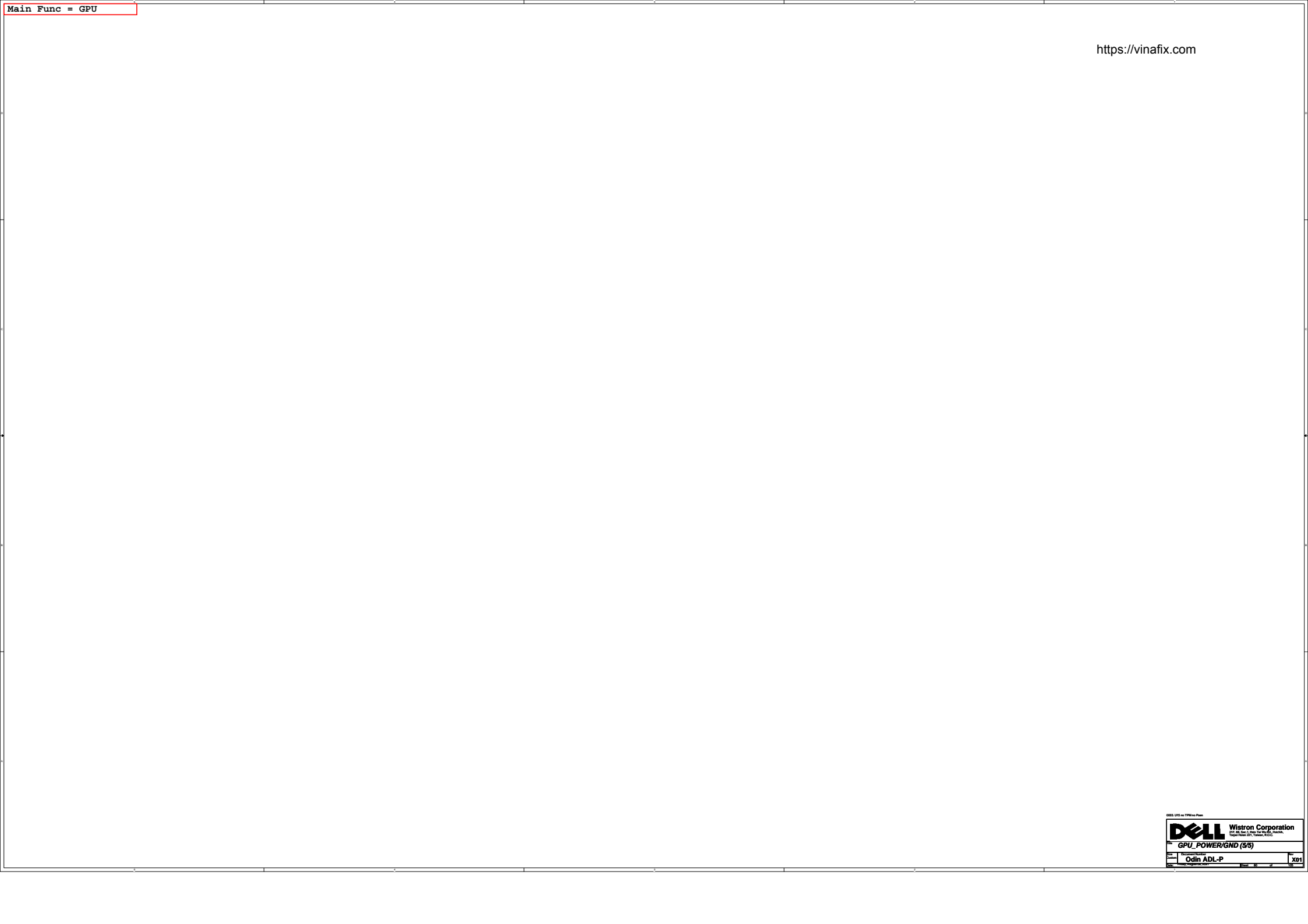
<https://vinafix.com>

0003. U15 no TPM no Psan

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Title					
<b>GPU DIGITALOUT (2/5)</b>					
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Main Func = GPU

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0003, 010 to 1199 are Pallets



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GPU\_POWER/GND (5/5)

Odin ADL-P

X01





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0003. U15 no TPM no Psen

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Title <b>VGA Power A</b>					
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0003. U15 no TPM no Psen

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>VGA Power B</b>					
Size A4		Document Number <b>Odin ADL-P</b>			Rev <b>X01</b>
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Main Func = dGPU

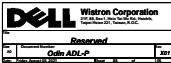
<https://vinafix.com>

0003. U15 no TPM no Psen

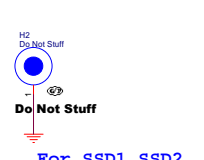
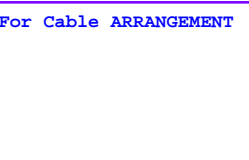
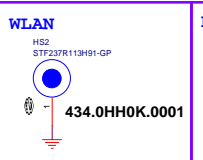
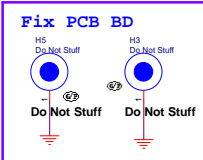


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Title			<b><i>Reserved</i></b>	
Size A3	Document Number		Rev	
	<b><i>Odin ADL-P</i></b>		<b><i>X01</i></b>	
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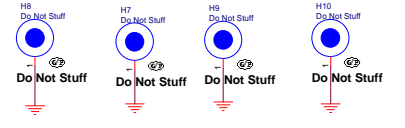


## Main Func = UnusedParts



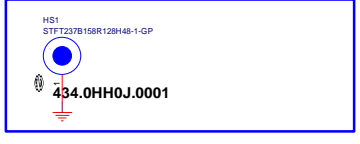
<https://vinafix.com>

### CPU SKREW HOLE



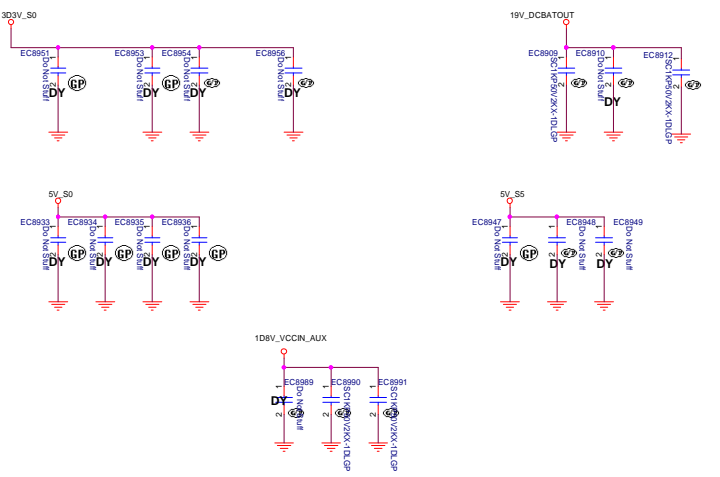
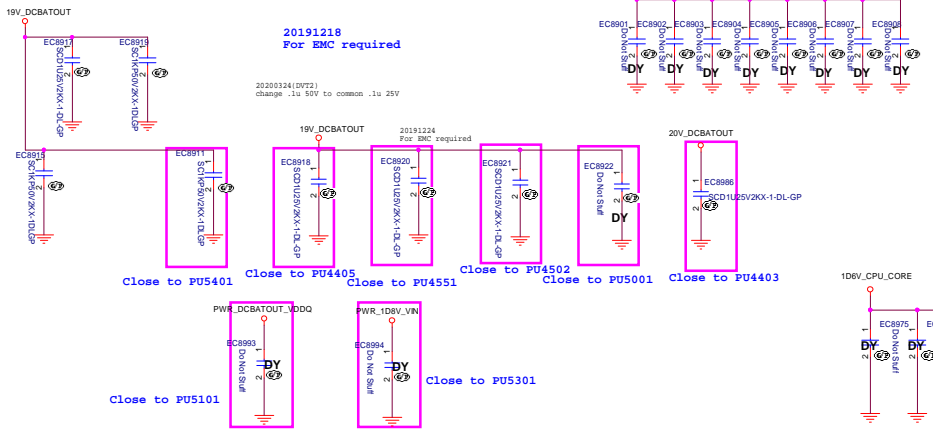
### GPU SKREW HOLE

### TYPEC SKREW HOLE



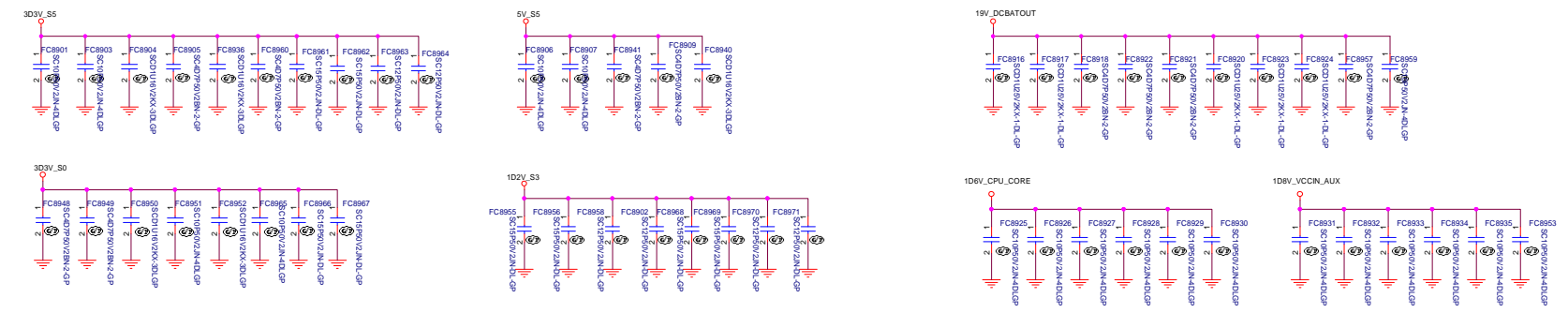
## Main Func = EMI Capacitors

Mind the voltage rating of the caps.



## Main Func = RF Capacitors


Mind the voltage rating of the caps.



0003, U15 no TPM no Psen

(Blanking)

0003. U15 no TPM no Psen



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## Main Func = TPM

```

17,26,39,61,63,71,75    PLT_RST_N    >>>_____

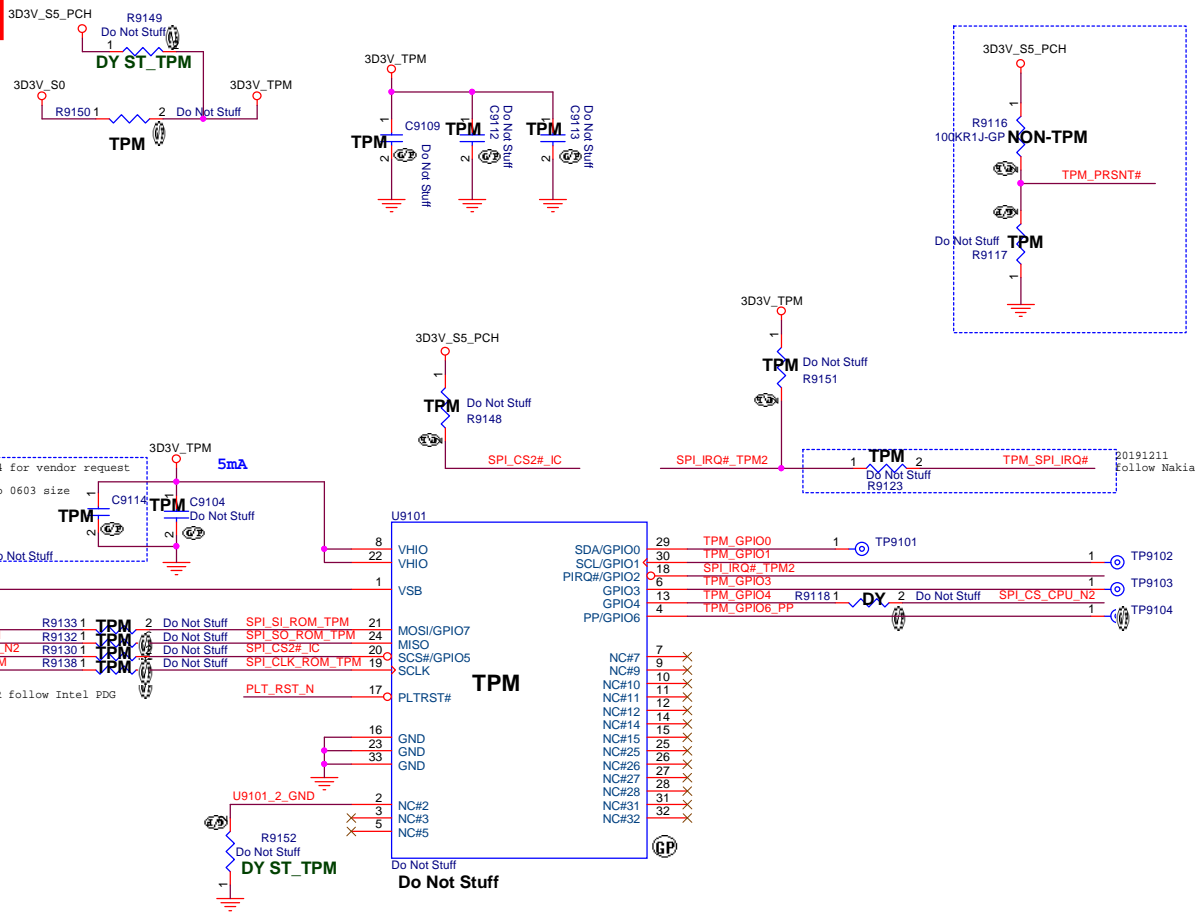
18,24,25,68             SPI_CLK_ROM   >>>_____
18,24,25,68             SPI_SI_ROM    >>>_____
18,24,25,68             SPI_SO_ROM    <<<_____

19    TPM_SPI_IRQ#      >>>_____

17    TPM_PSRNT#        <<<_____

18    SPI_CS_CPU_N2     >>>_____

```



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0003. U15 no TPM no Psen



SSID = Finger Print

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SSID = Finger Print

FPR Move to IOBD



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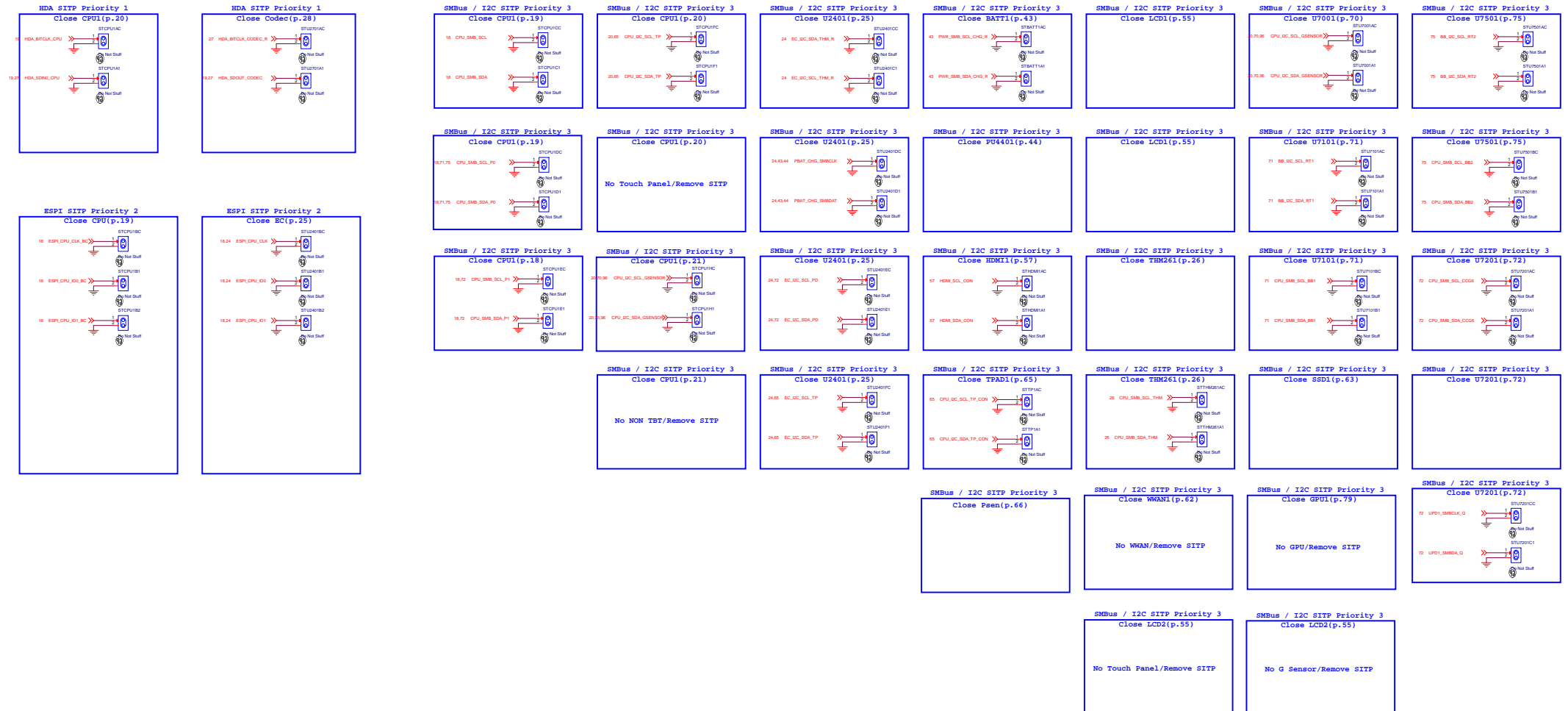
0003. U15 no TPM no Psen

		<b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title <b>(Reserved)</b>			
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Title

***LVDS\_Switch***

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**Odin ADL-P**

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**X01**

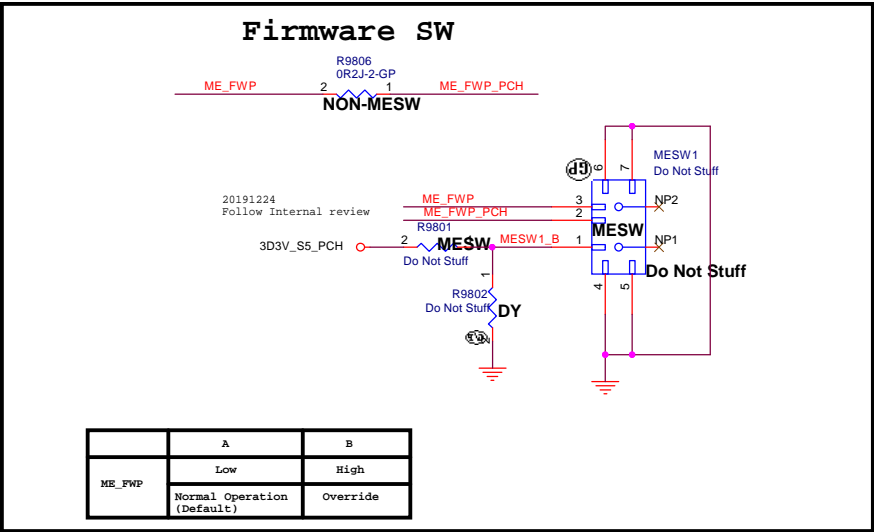
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Main Func = Firmware SW

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15 ME\_FWP\_PCH >>>  
24 ME\_FWP <<<



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Title			<b>CRT Switch</b>	
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0003. U15 no TPM no Psen

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Title			<b><i>Debug (XDP debug)</i></b>		
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TBD



*Change notes -*

[illegible]

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Title

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## (BTG) 808X BATT BTC

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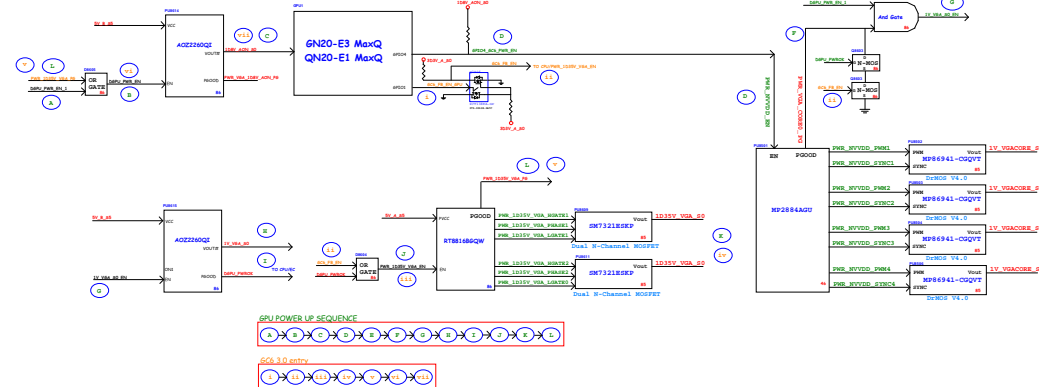
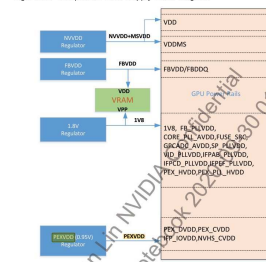
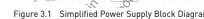
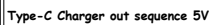


Figure 496. Alder Lake Non-DSx System Architecture Block Diagram

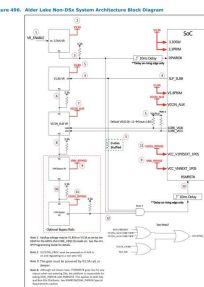


Figure 439. PWROK Generation Flow Diagram

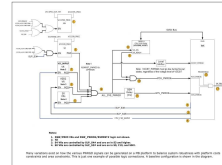


Figure 502. Timing Diagram for G3 to S5 [Non-Deep Sx Platform]

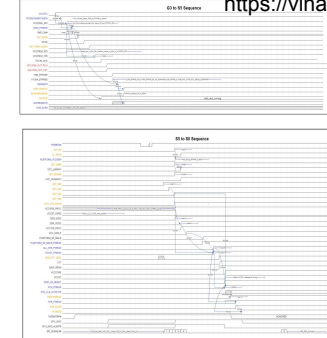


Figure 506. Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]

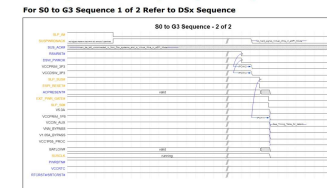
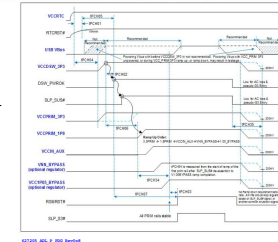
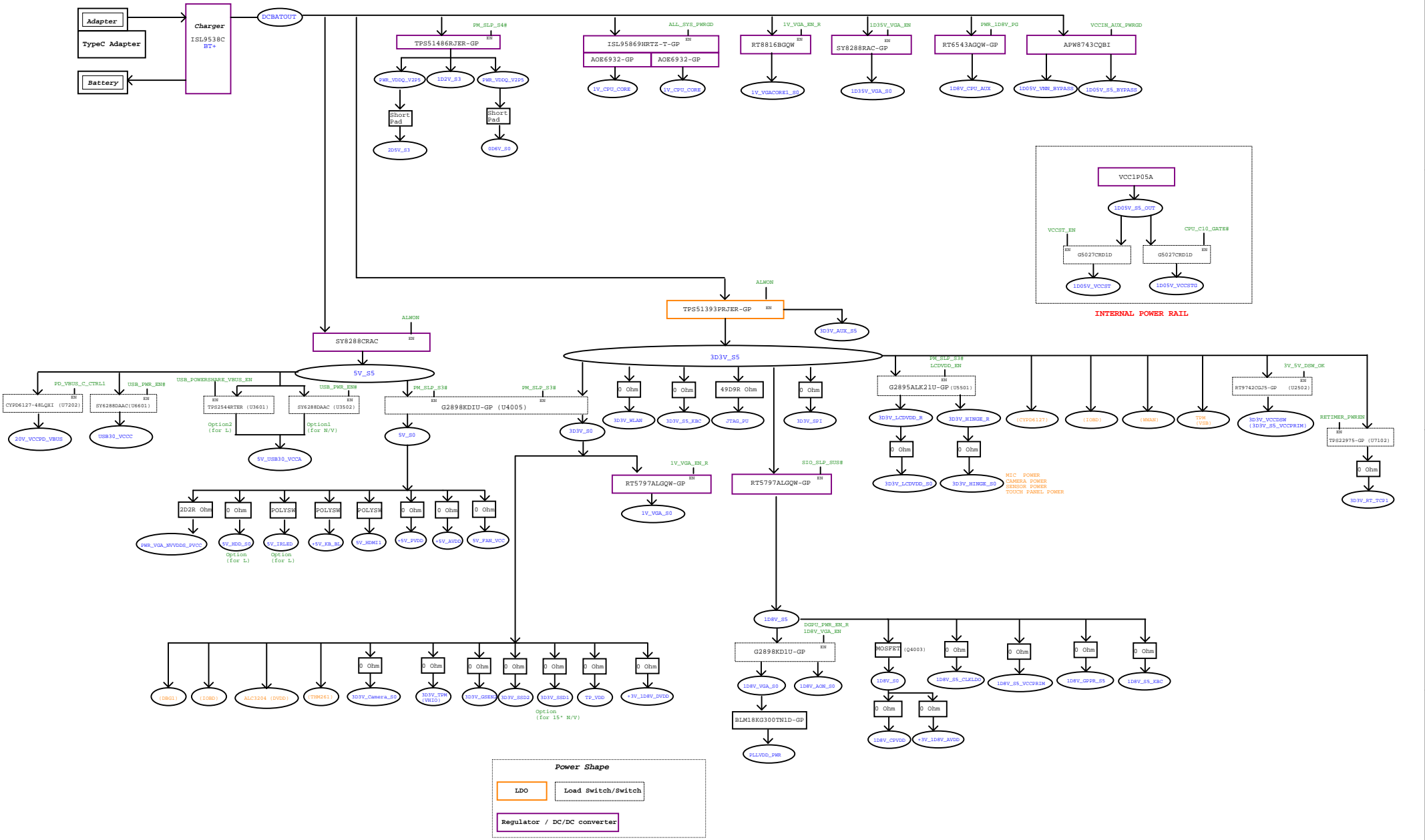


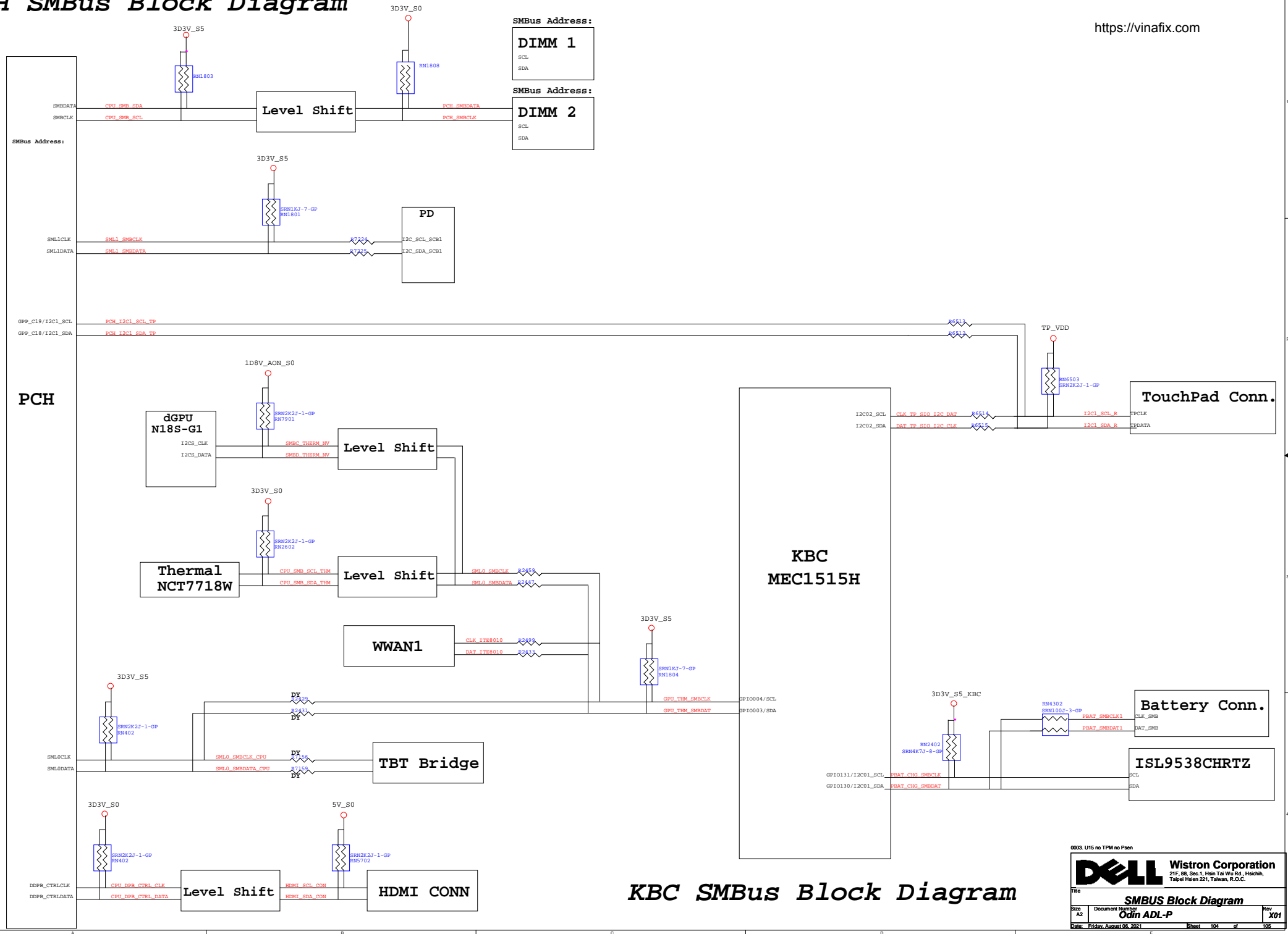
Figure S10. Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System





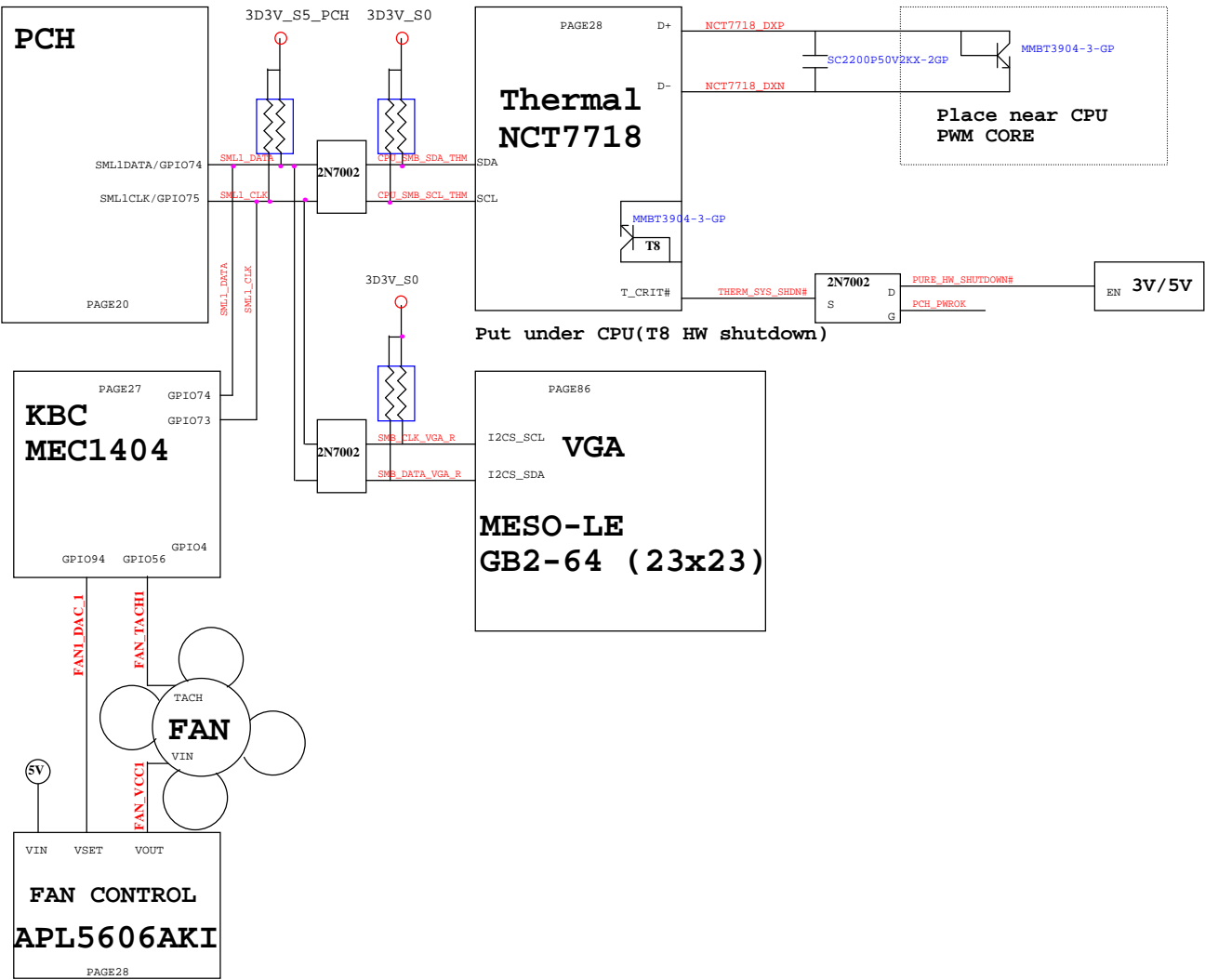
# PCH SMBus Block Diagram

<https://vinafix.com>



## KBC SMBus Block Diagram

# Thermal Block Diagram



# Audio Block Diagram

